Synthesizing Code for GPGPUs from Abstract Formal Models

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Paper

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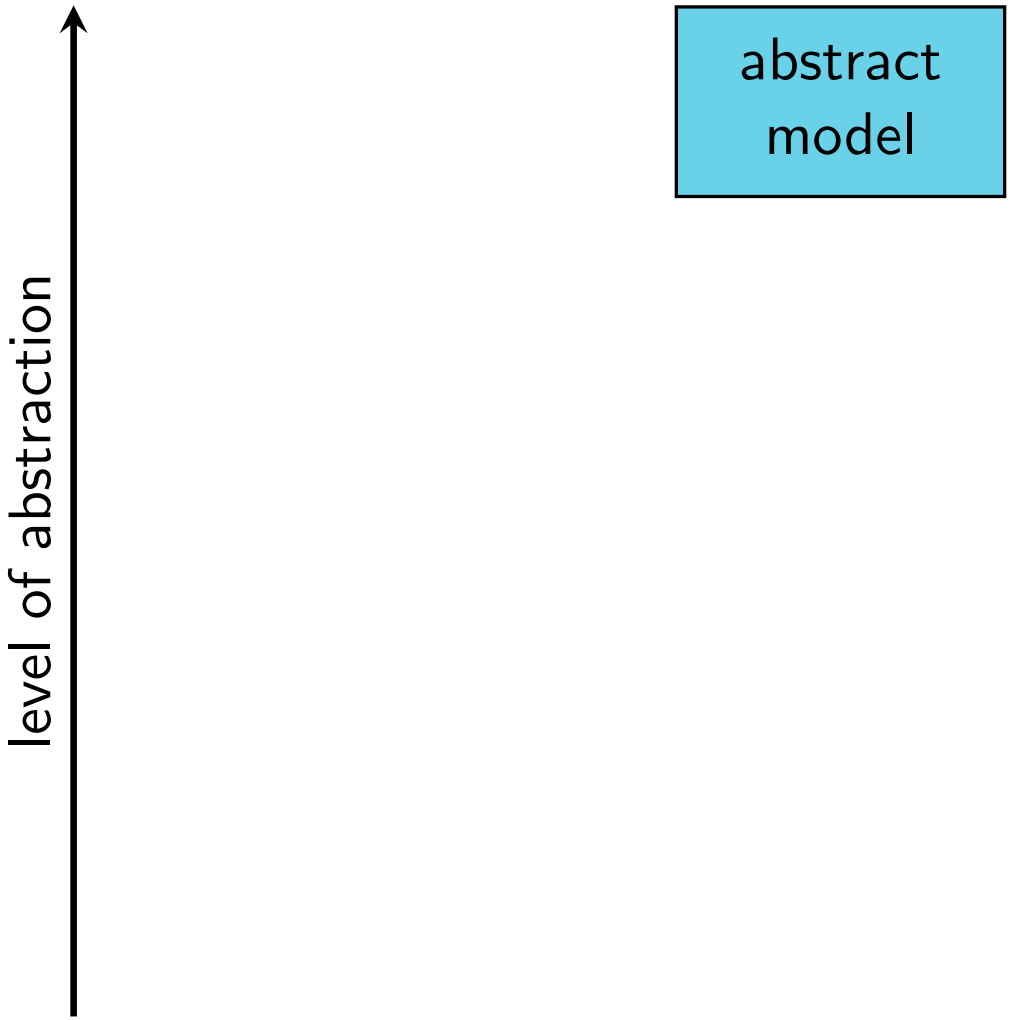
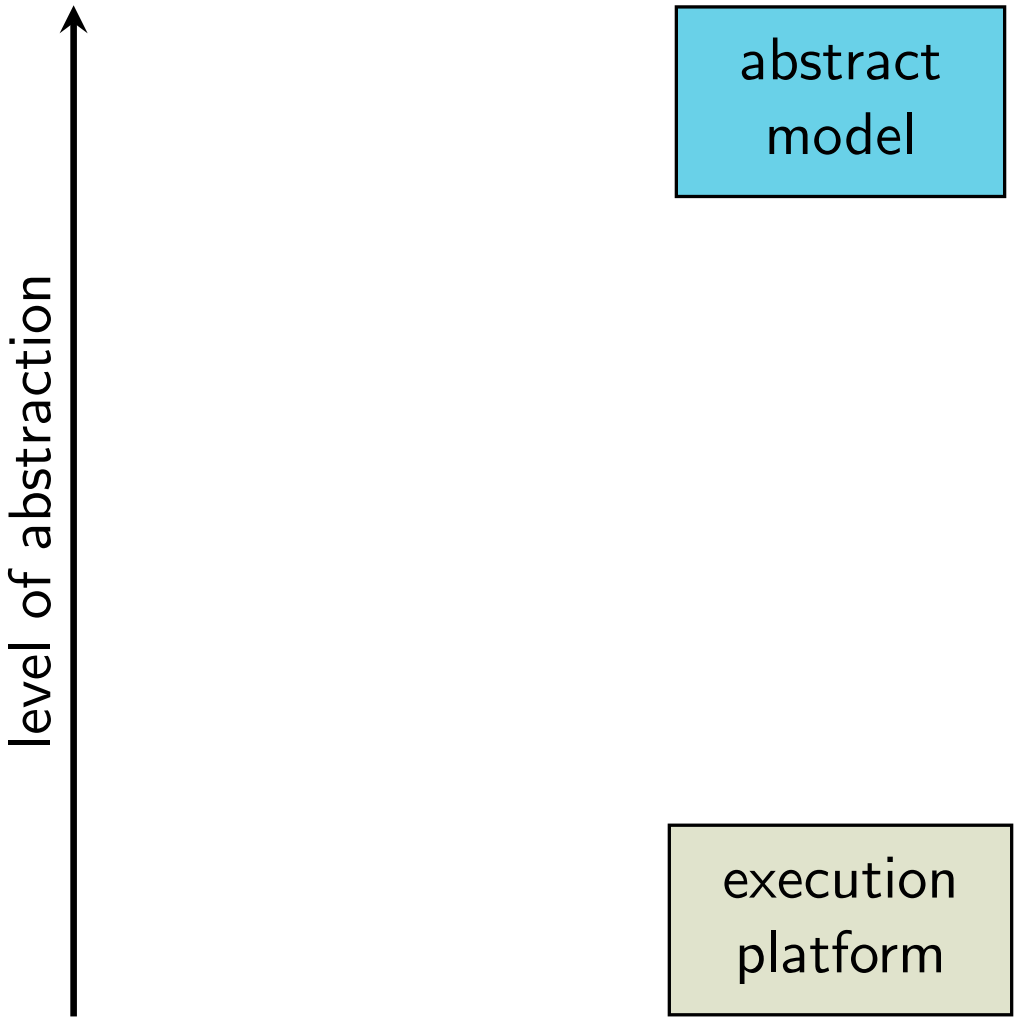
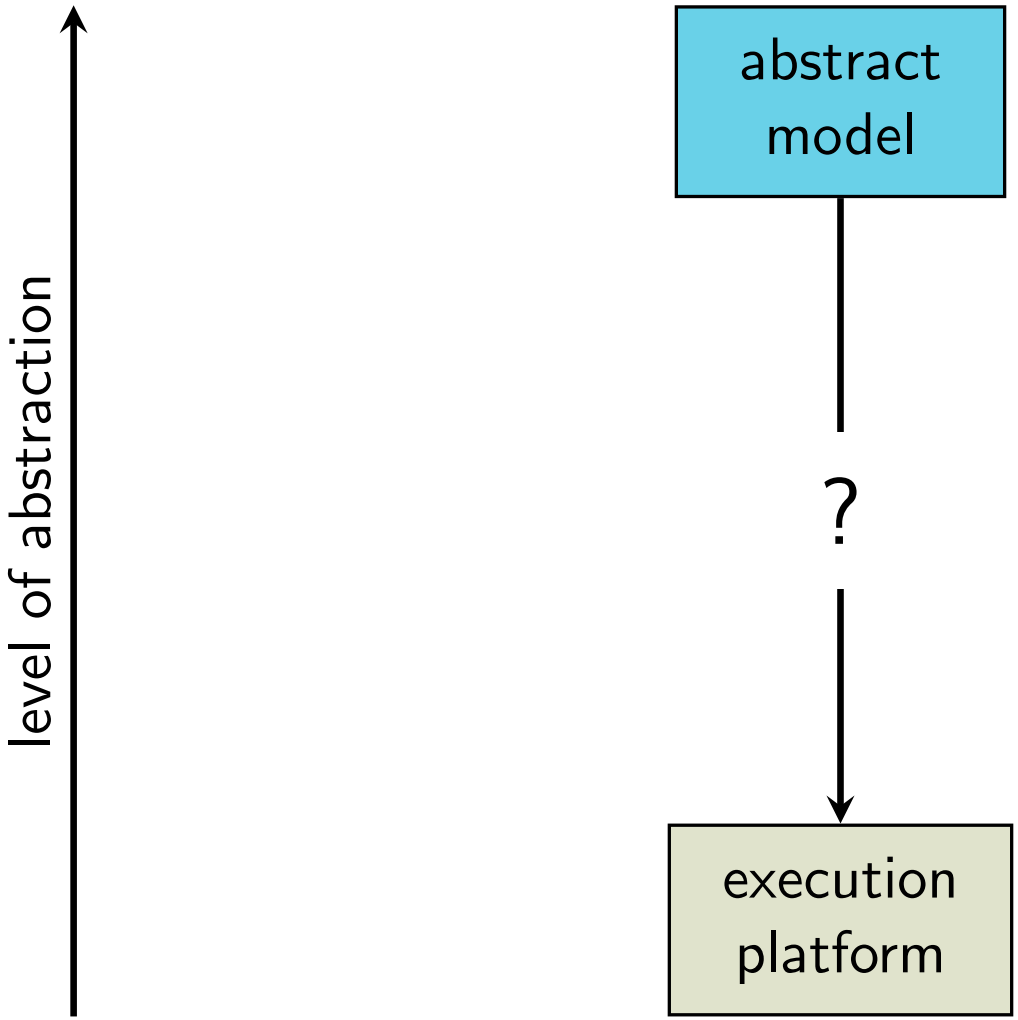
Ideal: Want to Model at a High Level of Abstraction



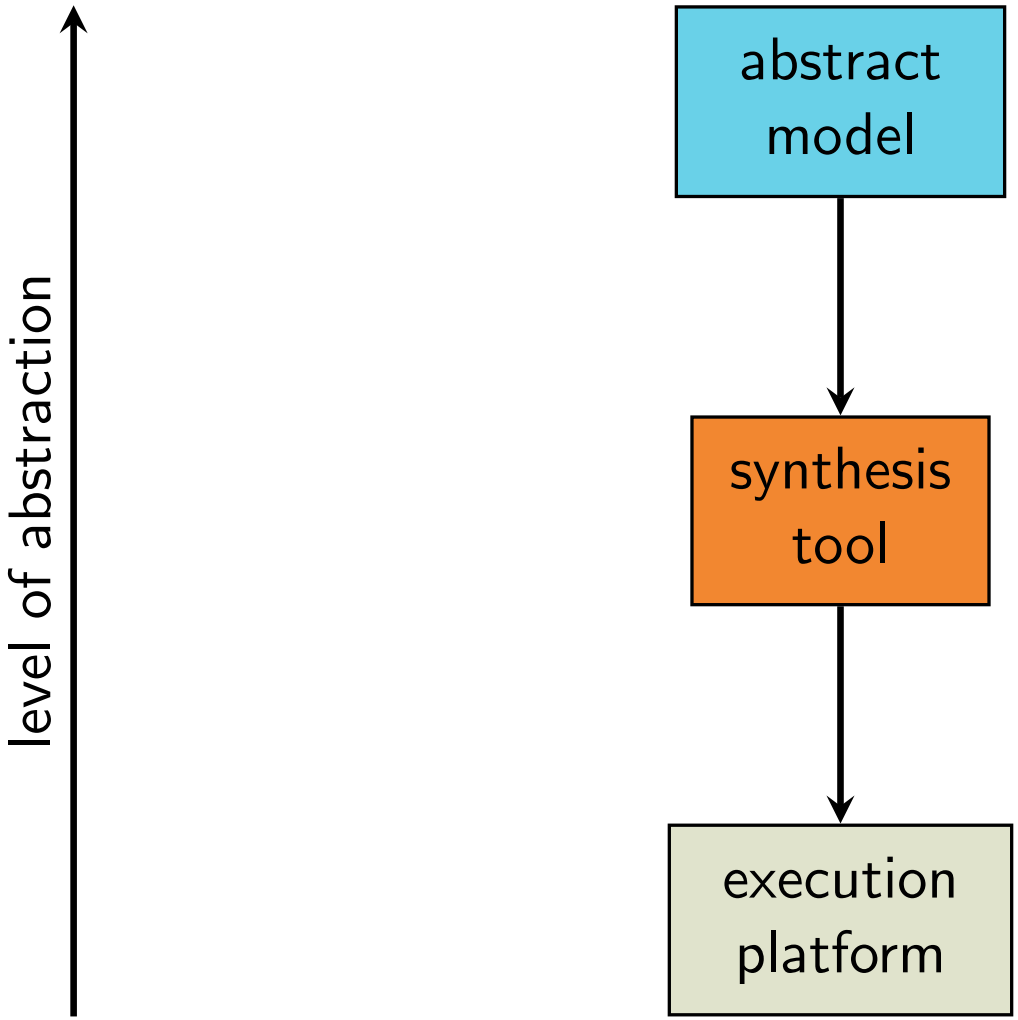
Reality: Have to Implement at a Low Level of Abstraction



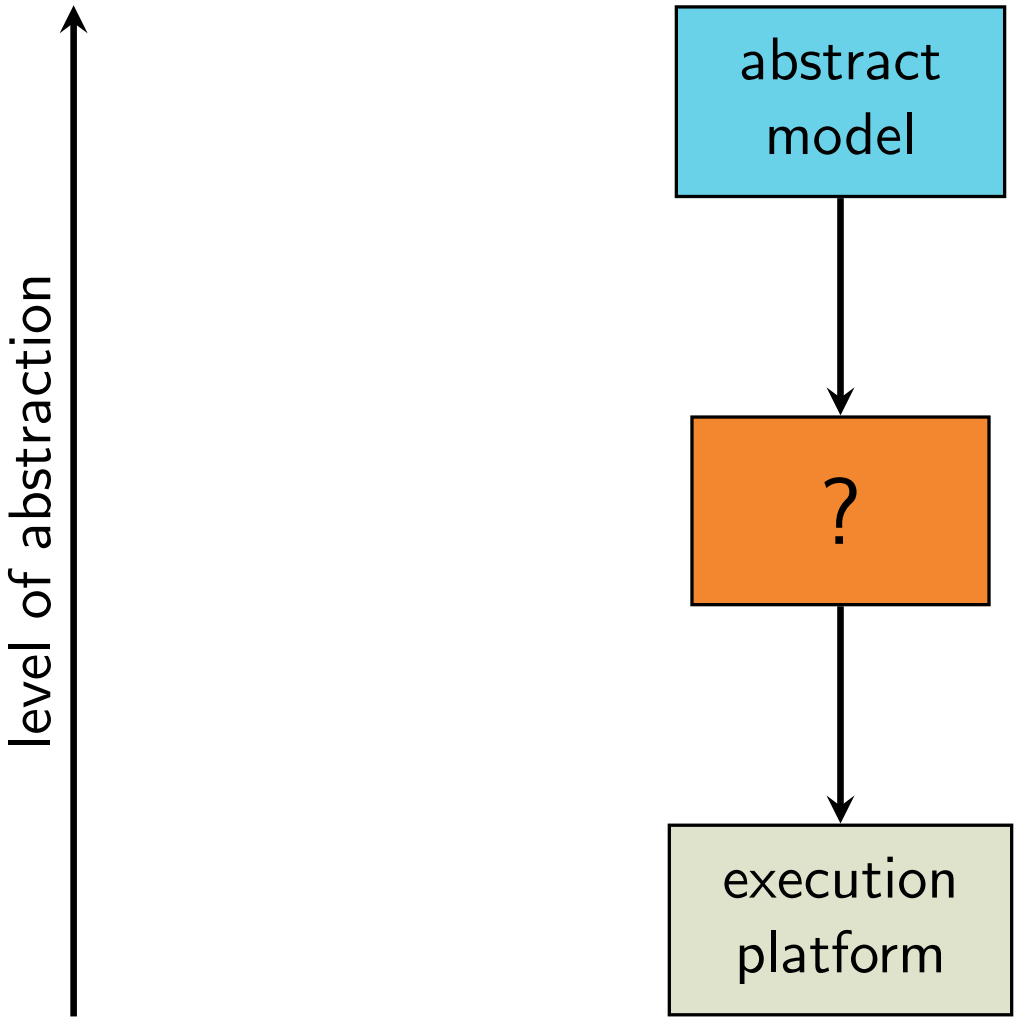
Problem: How to Bridge the Gap?



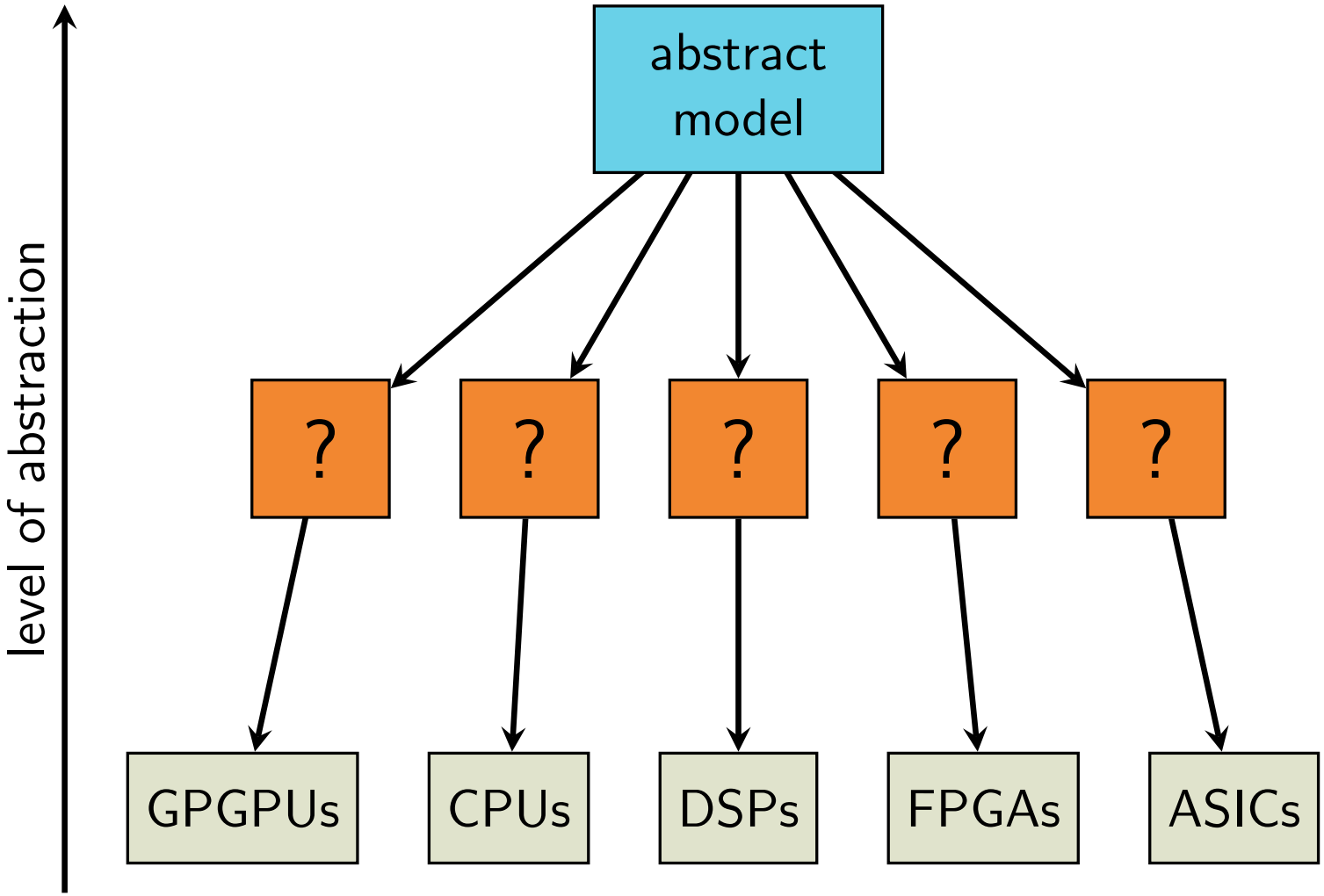
Solution: Use Automated Synthesis Tools



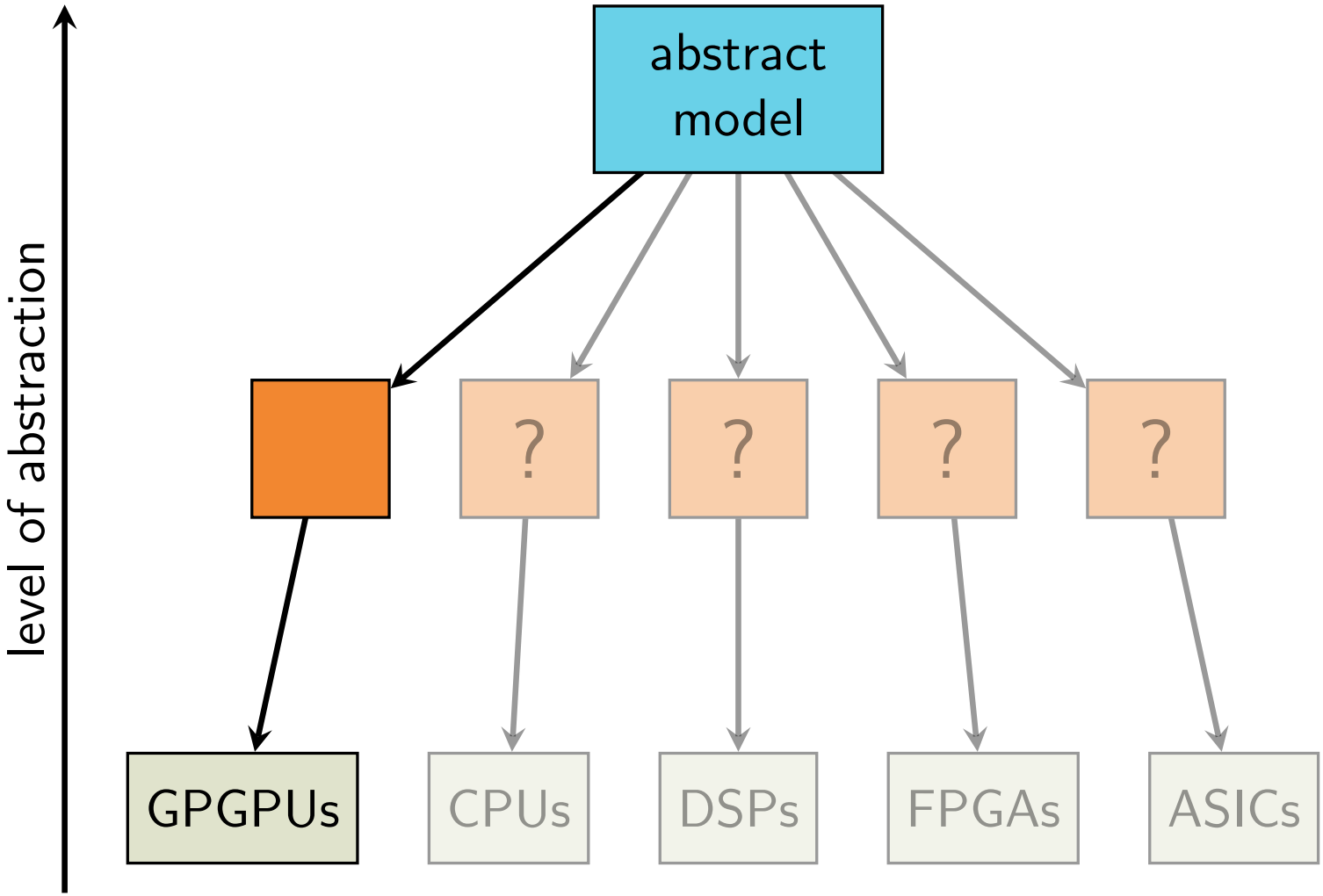
New Problem: How to Build Such a Tool?



New Problem: Different Challenges for Different Platforms



This Talk: A Synthesis Tool for GPGPUs



Outline

- Background
  - GPGPUs
  - ForSyDe
- Our ideas and synthesis tool (`f2cc`)
- Experiments
- Summary

What Are GPGPUs?

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- *General-Purpose Graphics Processing Unit*

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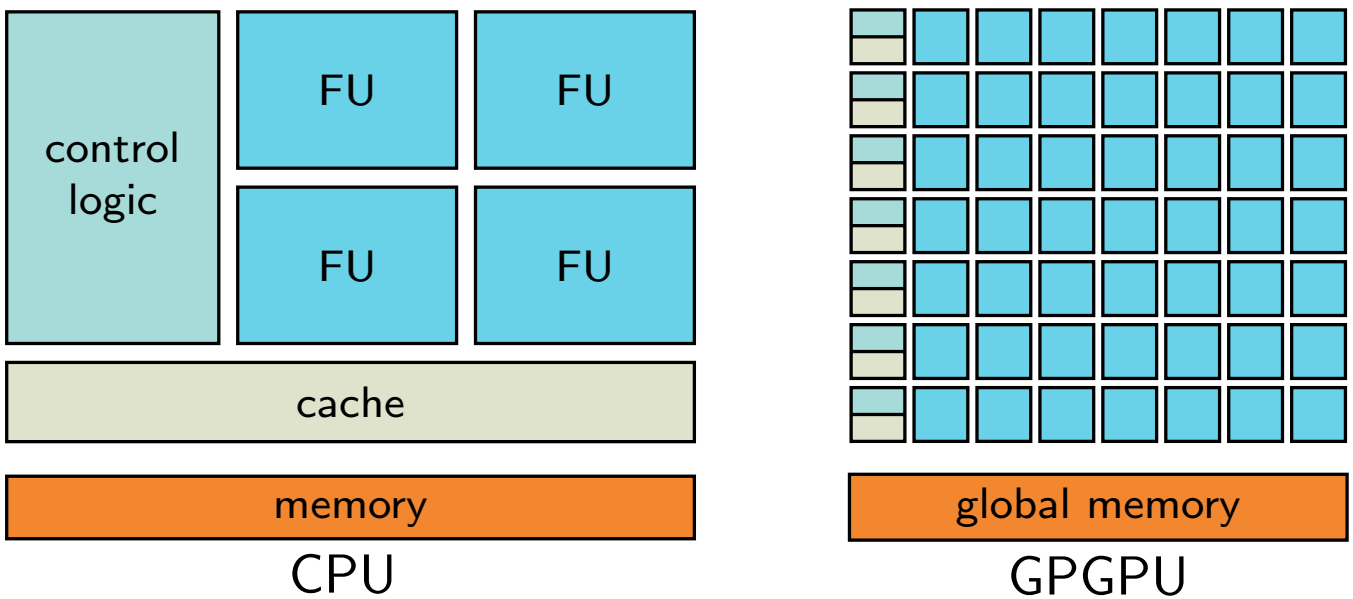
- *General-Purpose Graphics Processing Unit*
- Massively parallel, throughput-oriented platform
- Can yield tremendous speedup for data-parallel programs
- Comparison between CPUs and GPGPUs:



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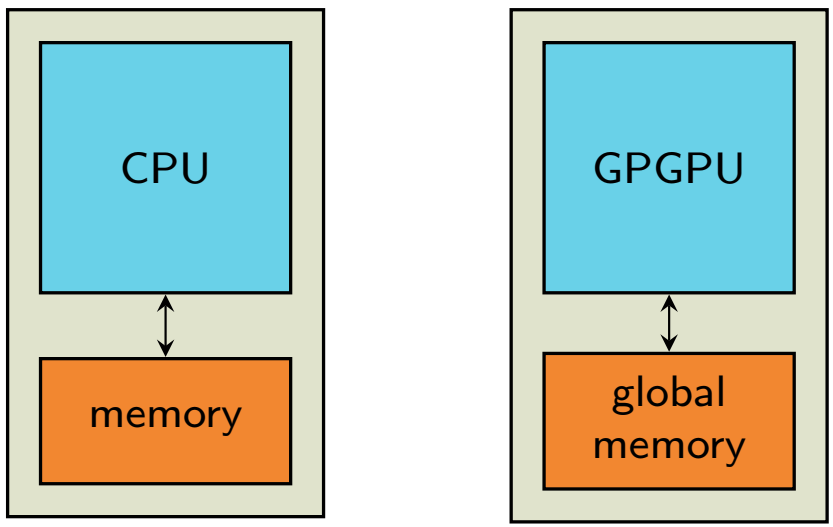

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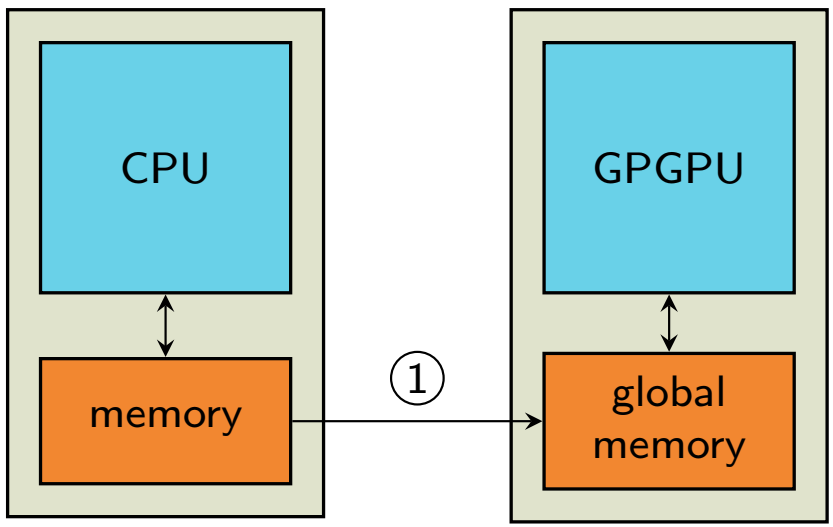
```
cudaMalloc(...);
cudaMemcpy(&data);
```



Copy input data

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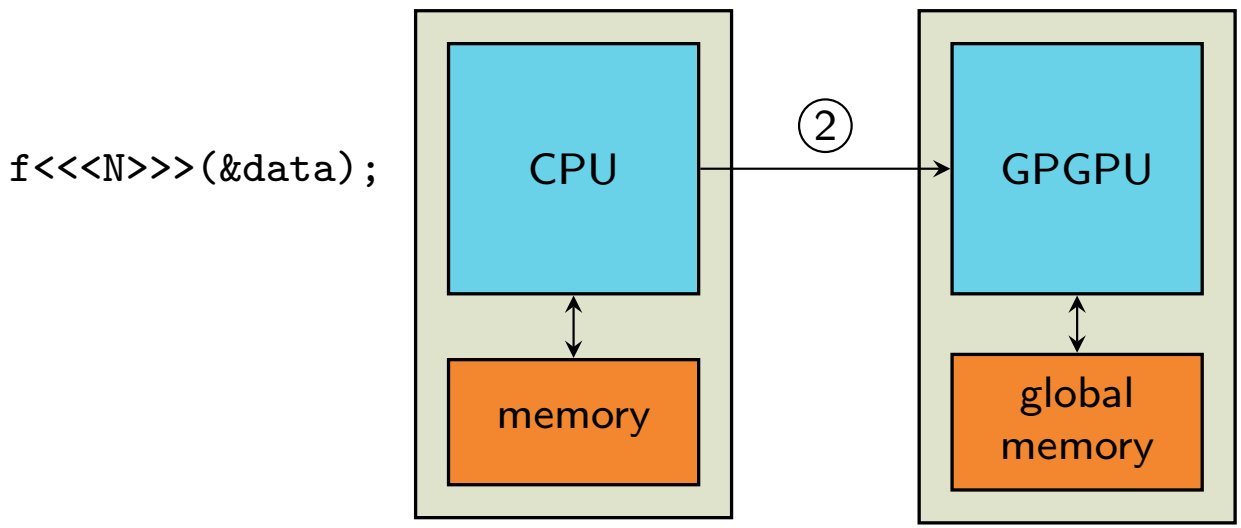

Tell GPGPU to execute function f on input data, using N threads

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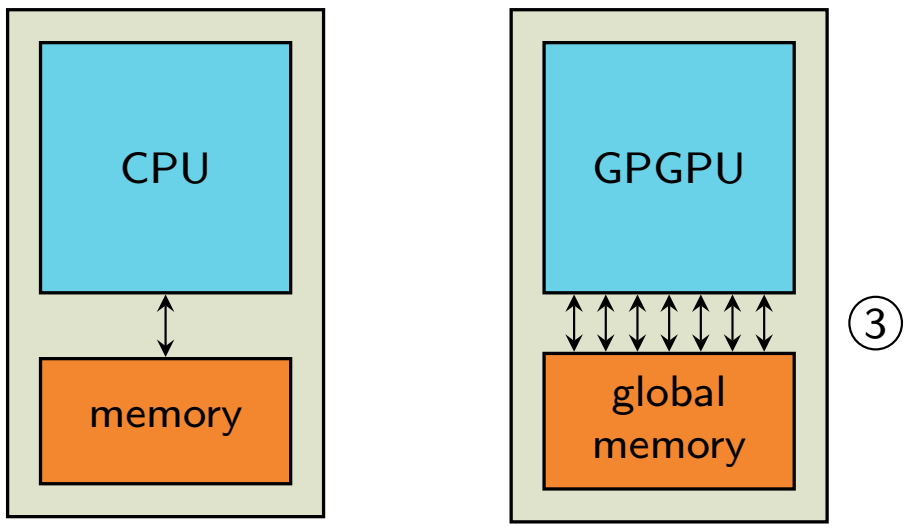
```
while (1);
```



Wait until all threads have finished

How to Use GPGPUs?

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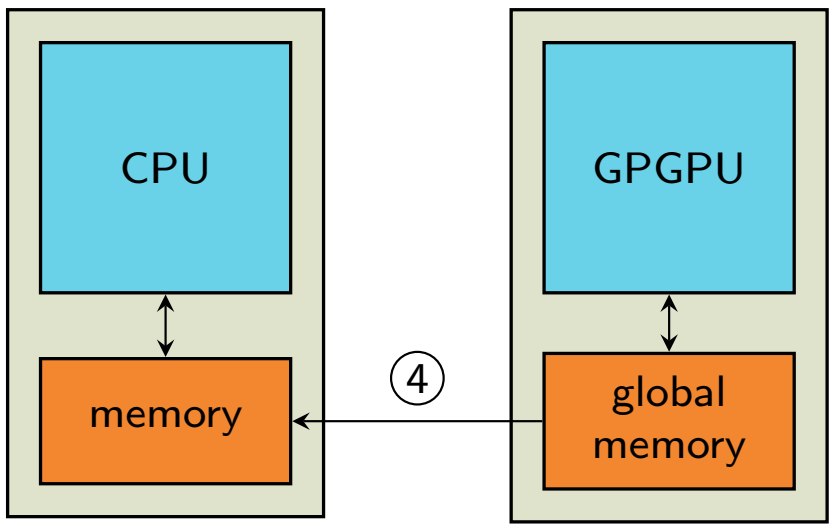
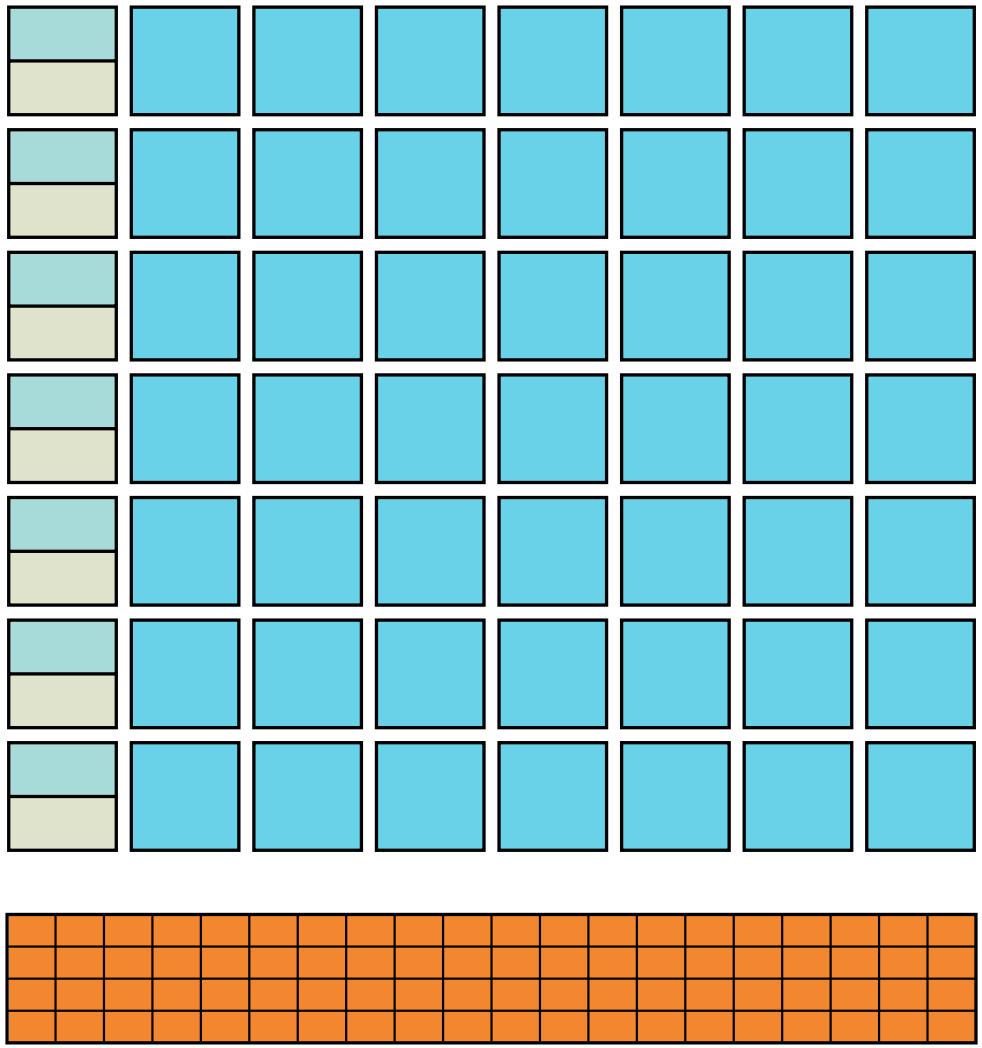
```
cudaMemcpy(&res);
cudaFree(...);
```

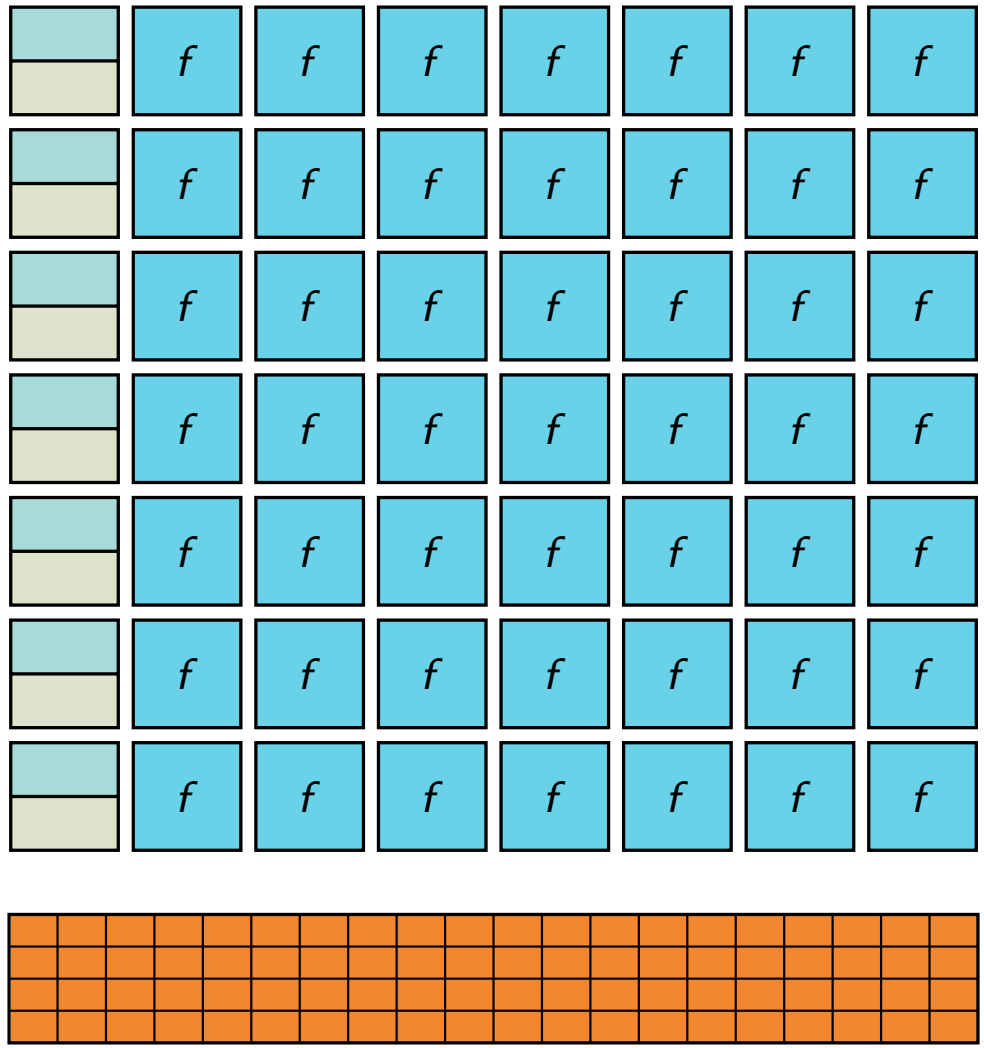


Copy result

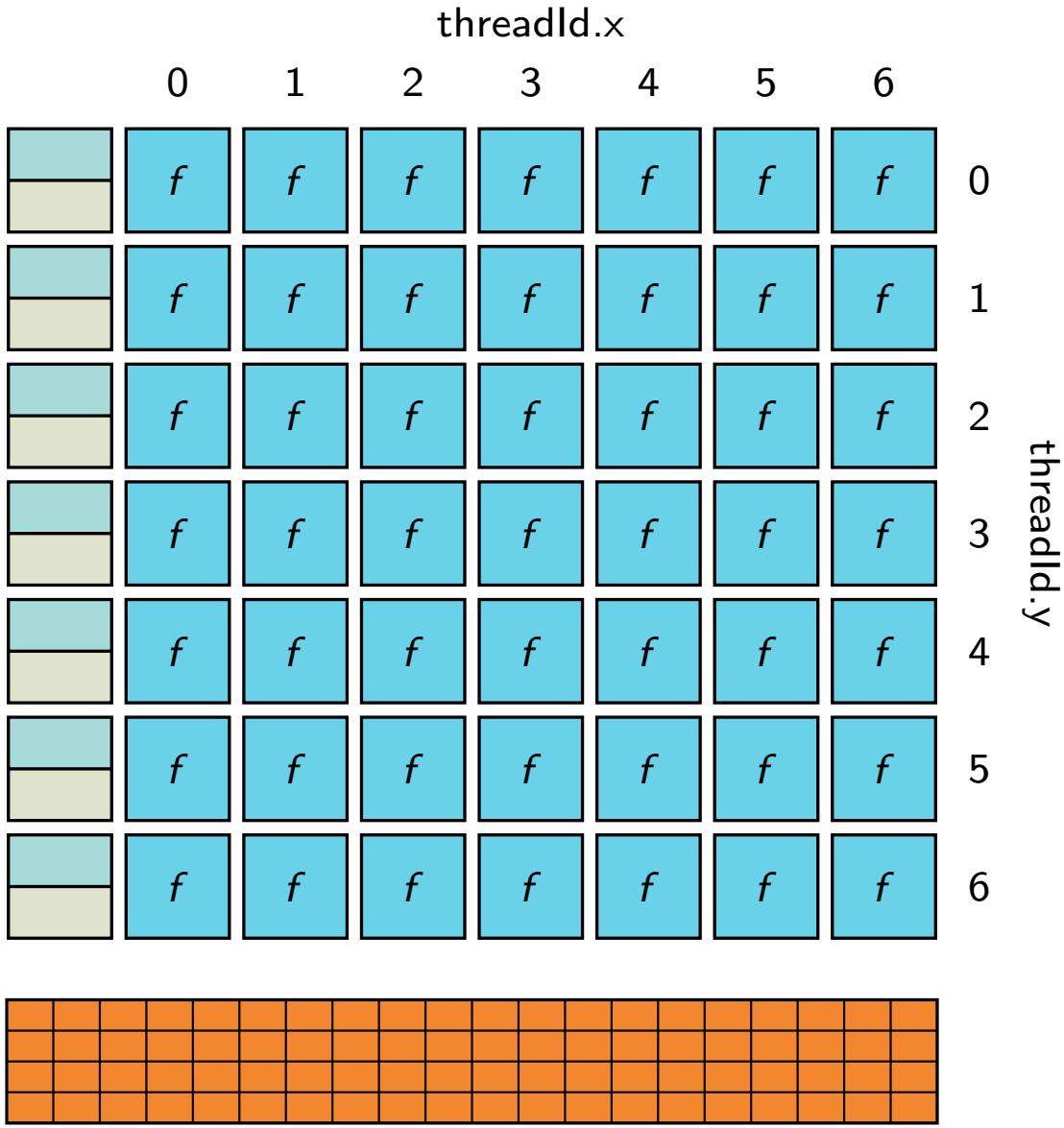
Inside the GPGPU During Execution



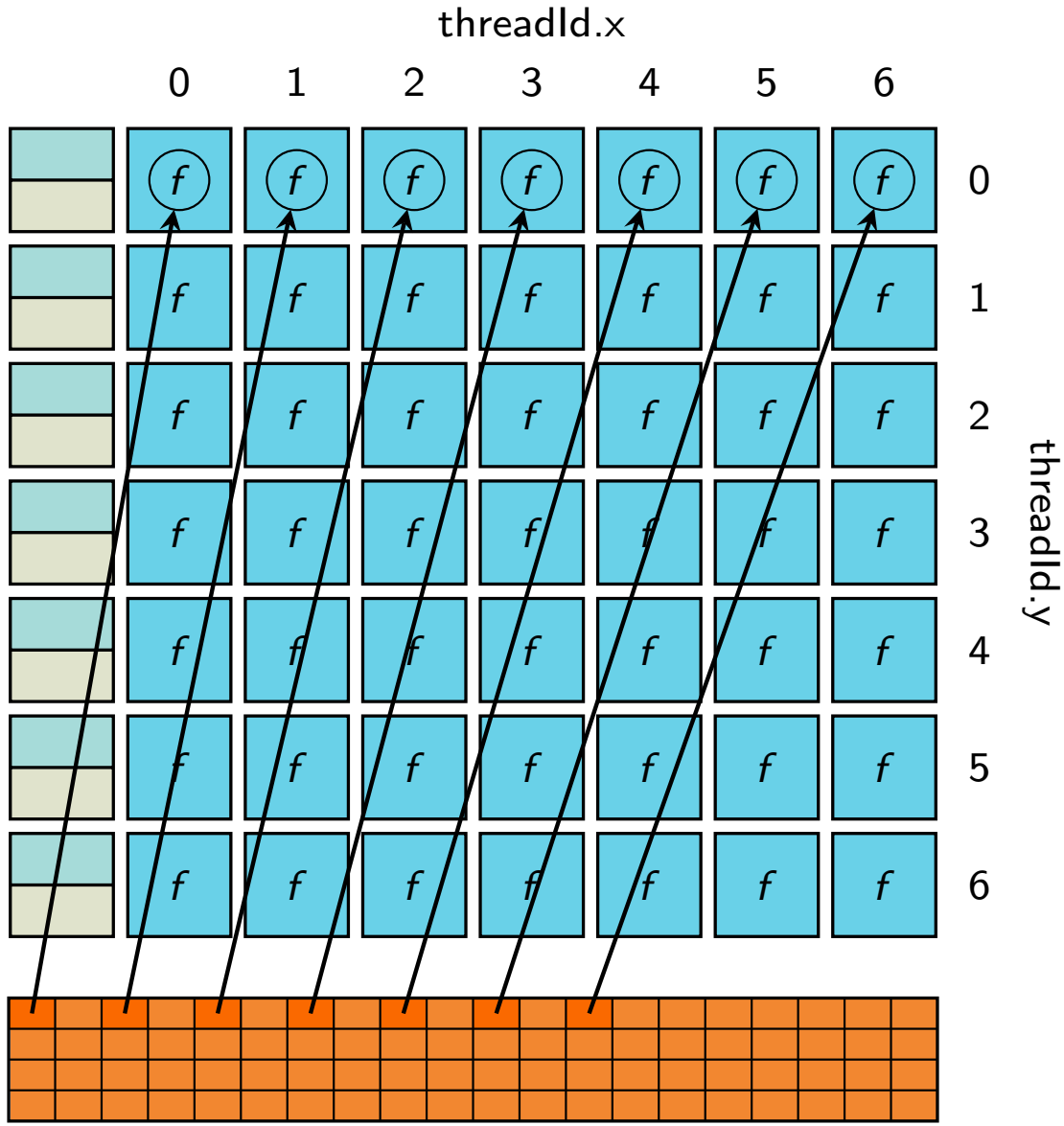
Every Thread Executes the Same f



Each Thread Has a Unique *Thread ID*



f Uses Thread ID to Determine What Data to Read



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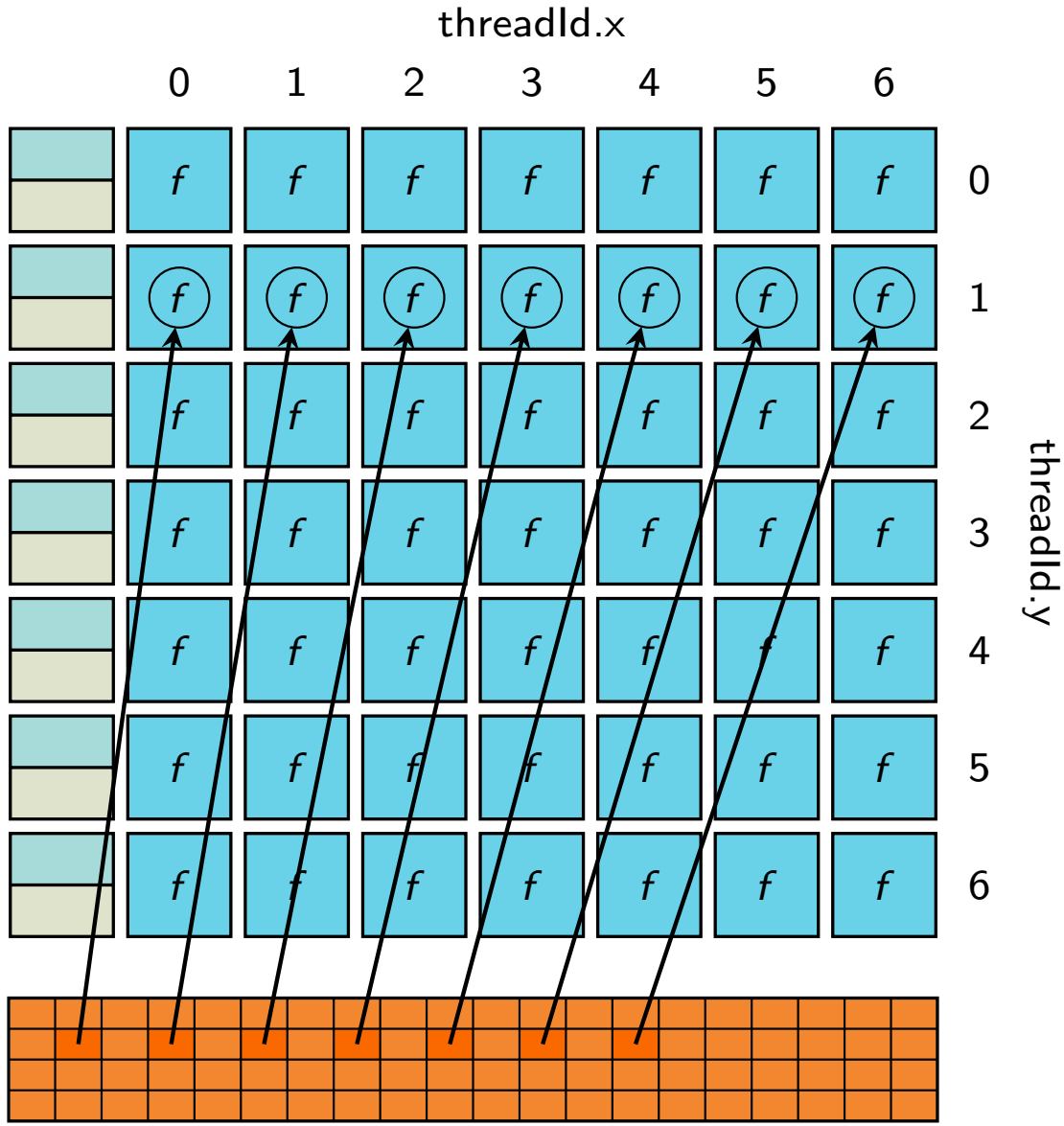

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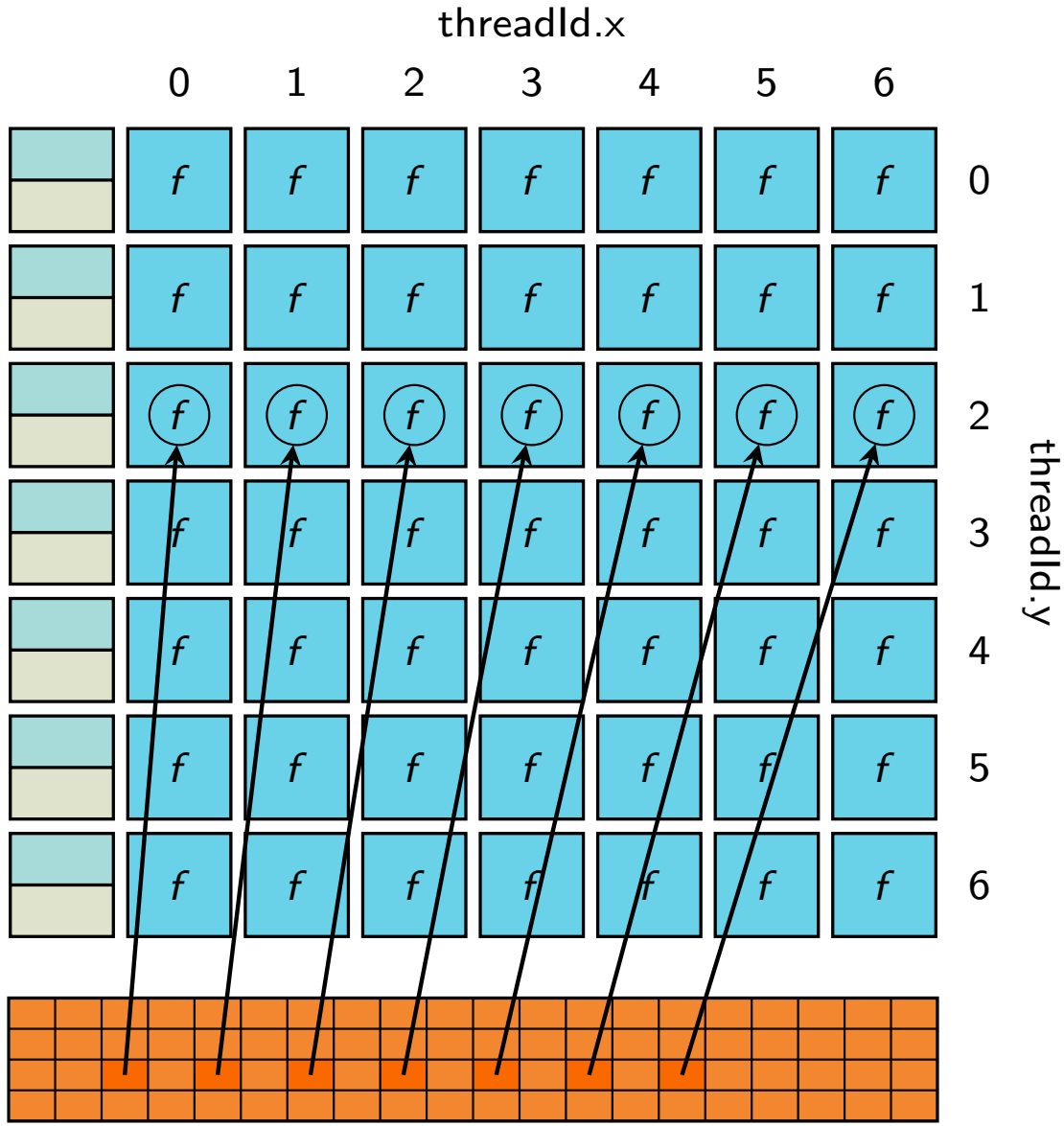
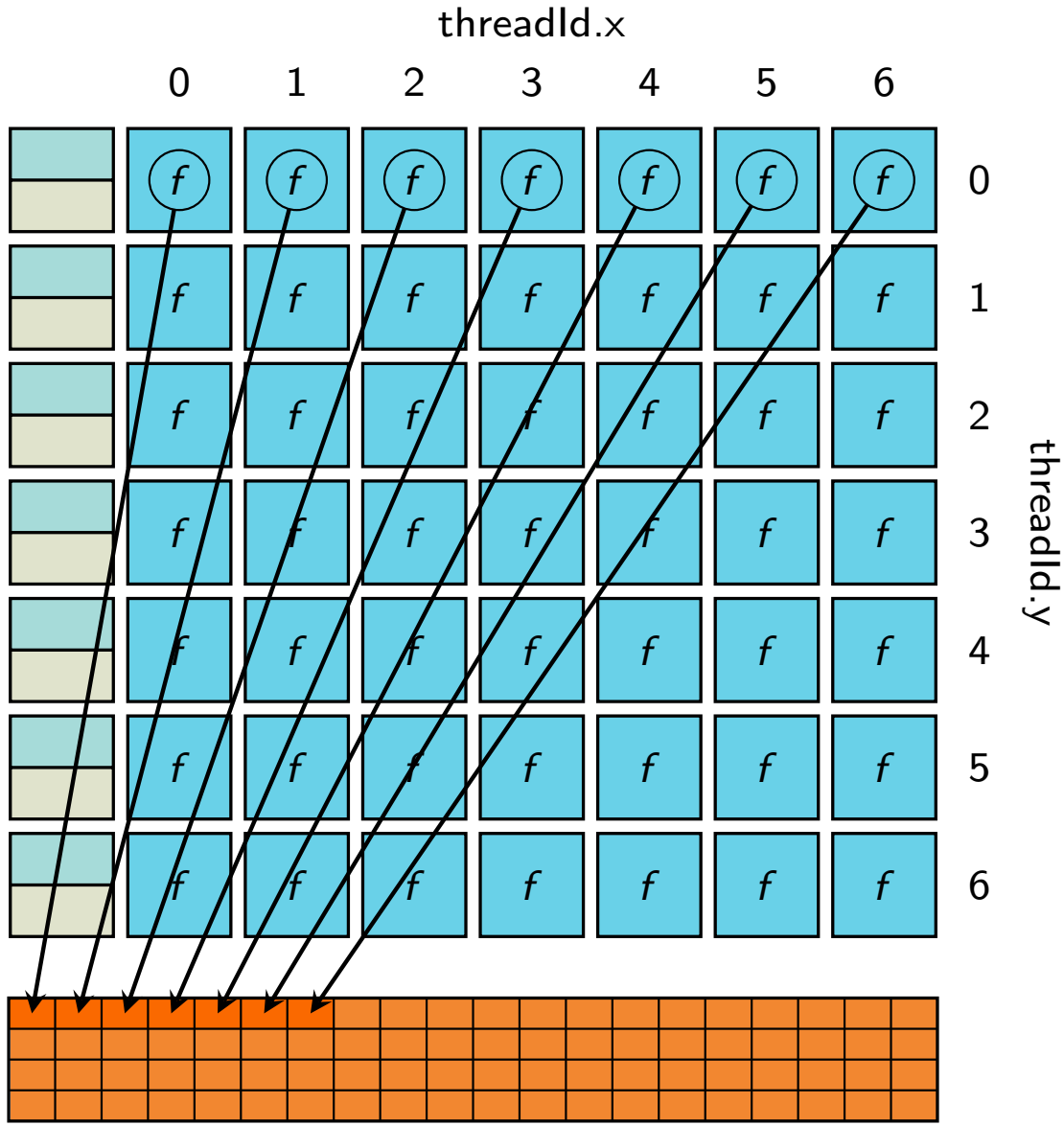


f Uses Thread ID to Determine Where to Write Results



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- Abundance of data parallelism to offset GPGPU overhead (due mainly for data copying)

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- High Computation-to-Global Memory Traffic Ratio
  - Often requires efficient use of various resources (like *shared memory*)
- No resource over-use

GPGPUs are Powerful, but Difficult to Program

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- Complex data indexing schemes

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- Complex data indexing schemes
- Performance depends on many interconnected factors

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- *Formal System Design*
- A formal modeling methodology
  - Uses the theory of *Models of Computation (MoCs)*
  - Captures behavior of heterogeneous embedded systems as *ForSyDe models*

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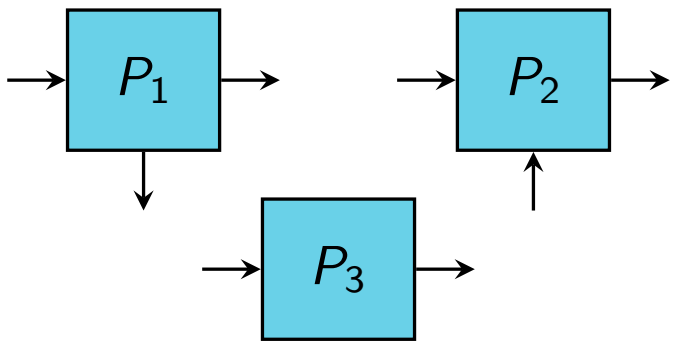
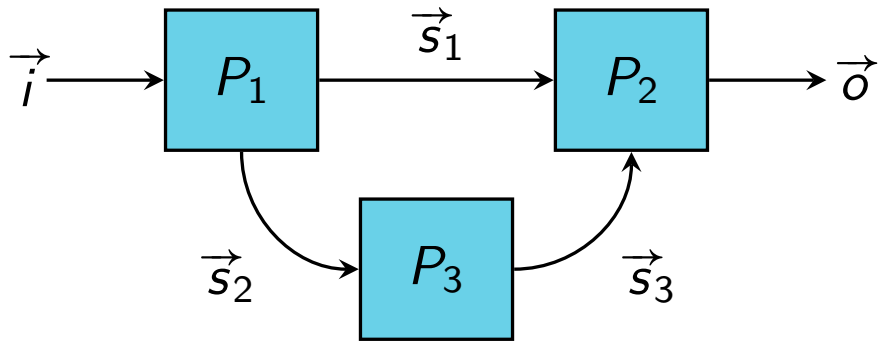


A ForSyDe model is a *concurrent network* of *processes* ...

What Is a ForSyDe Model?



. . . that communicate via *signals*.

What Is a Process Constructor?

What Is a Process Constructor?

process constructor

A process constructor is a *template* . . .

What Is a Process Constructor?

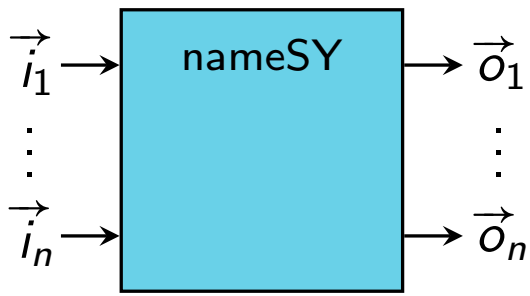
process constructor

based on the
synchronous MoC

. . . that is *based* on a specific model of computation, . . .

What Is a Process Constructor?

process constructor

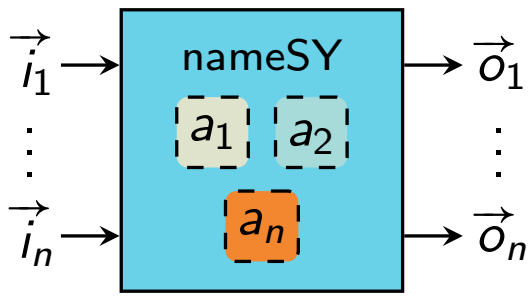


based on the
synchronous MoC

. . . has a number of declared *input* and *output signals*, . . .

What Is a Process Constructor?

process constructor



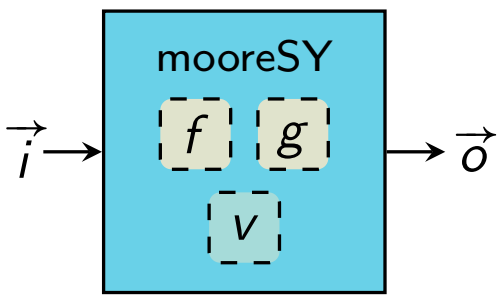
based on the
synchronous MoC

. . . and takes zero or more *side effect-free arguments*.

Creating a Process

Creating a Process

process constructor



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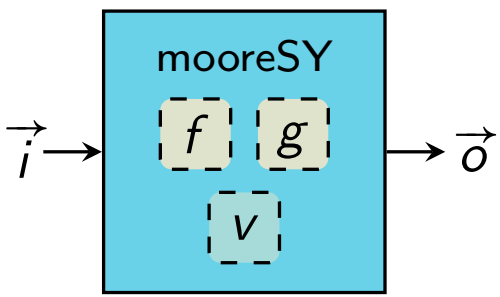
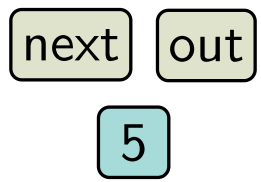


+

arguments



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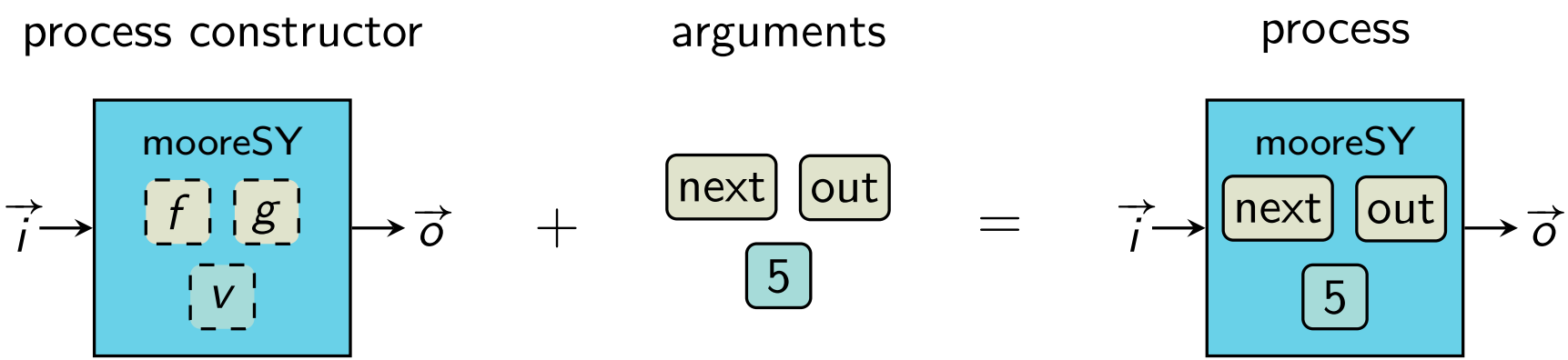
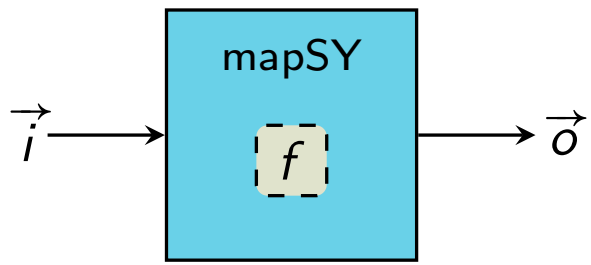


The MapSY Process Constructor



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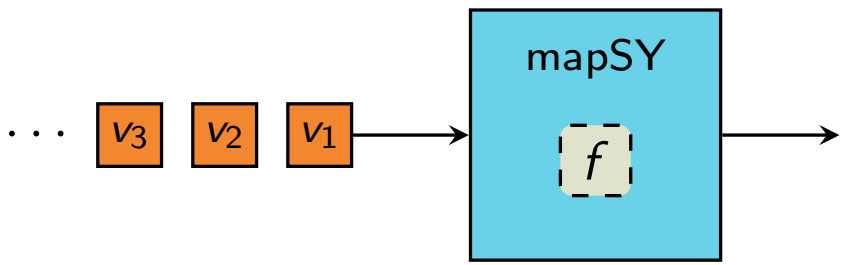

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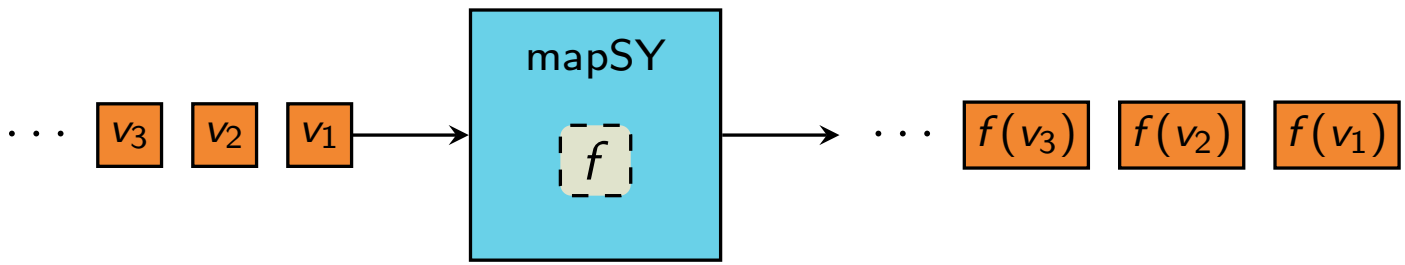
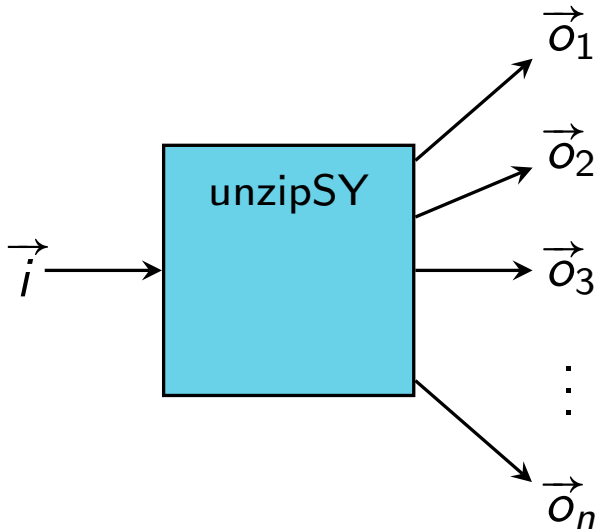


The UnzipSY Process Constructor



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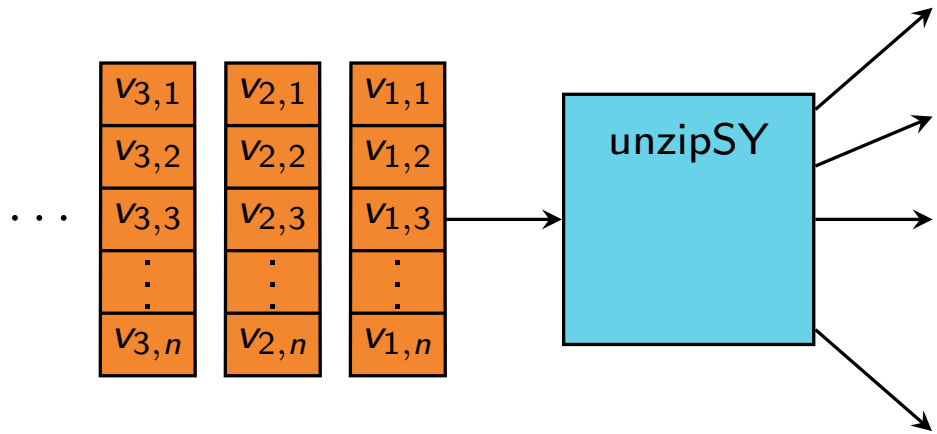

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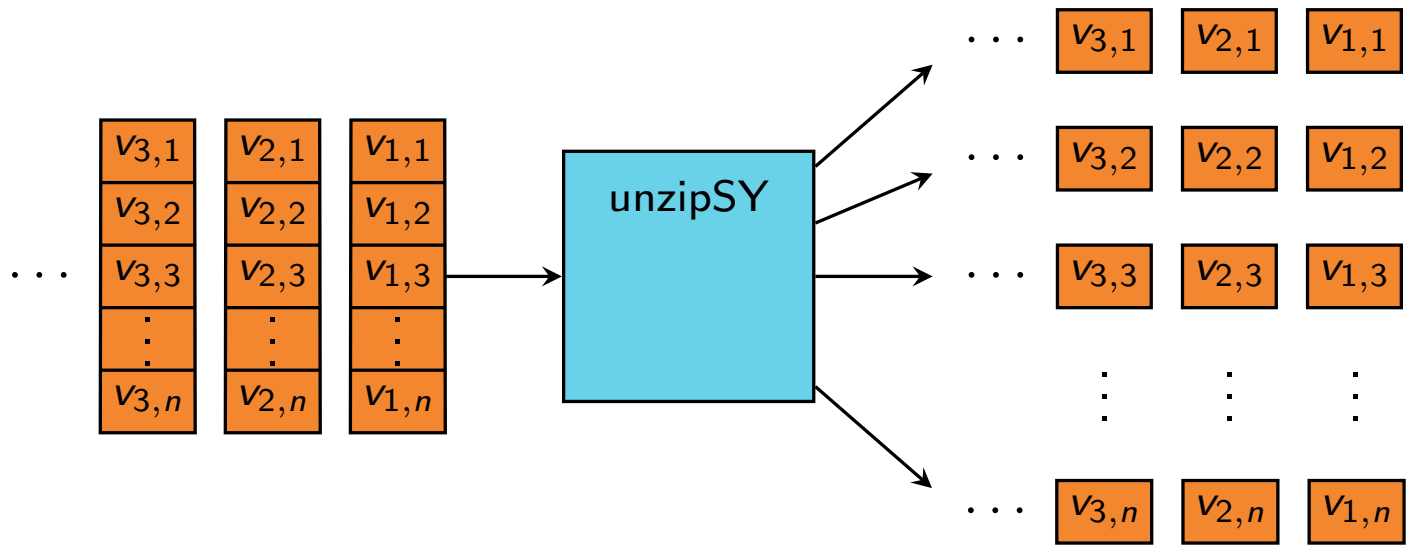

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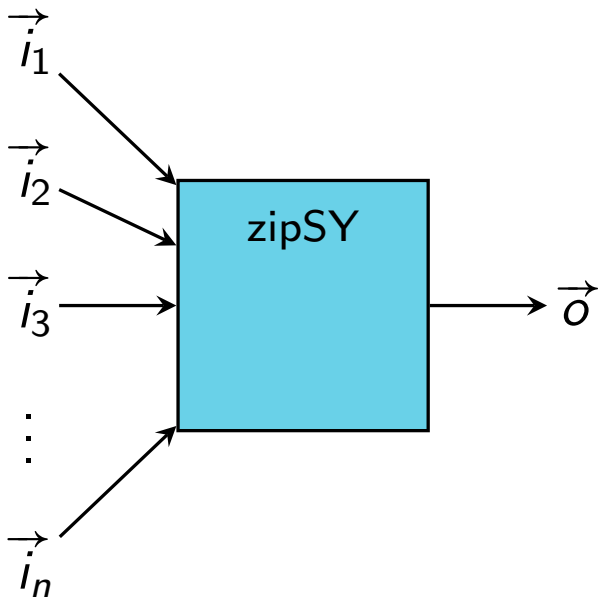

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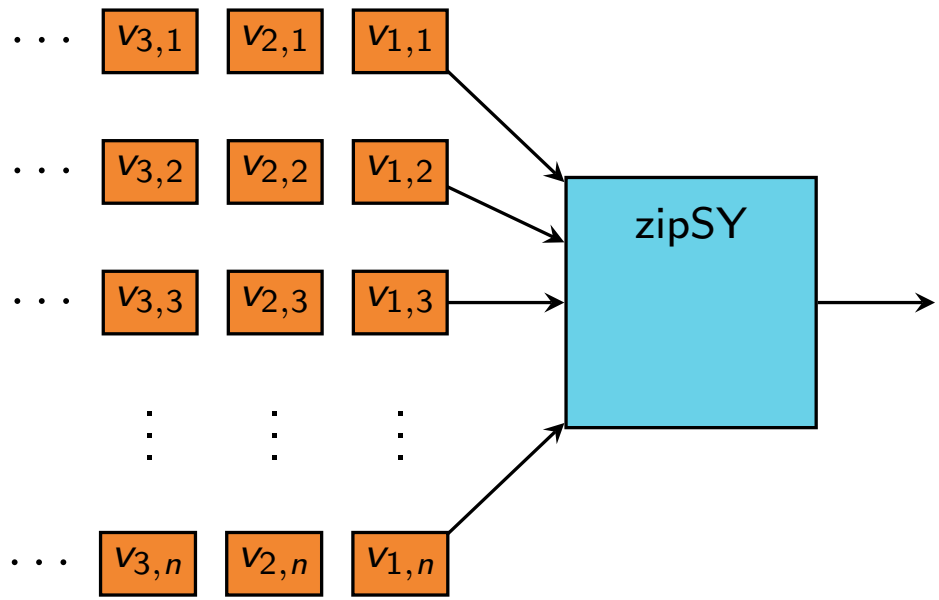

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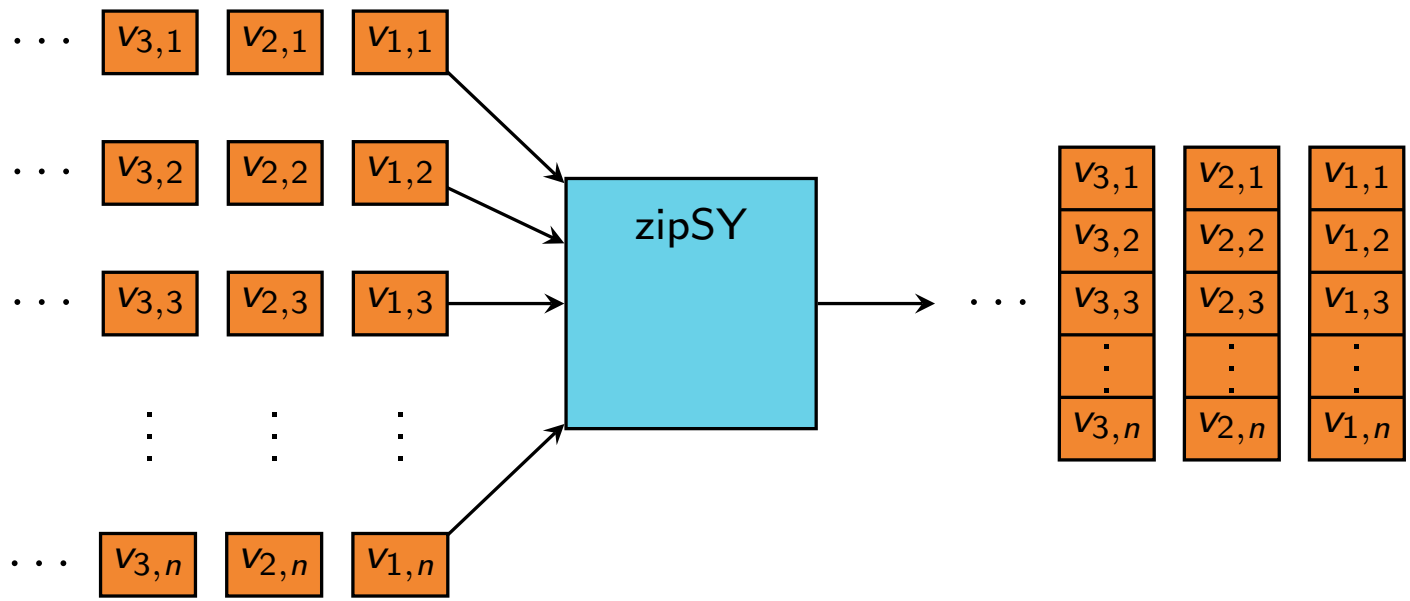

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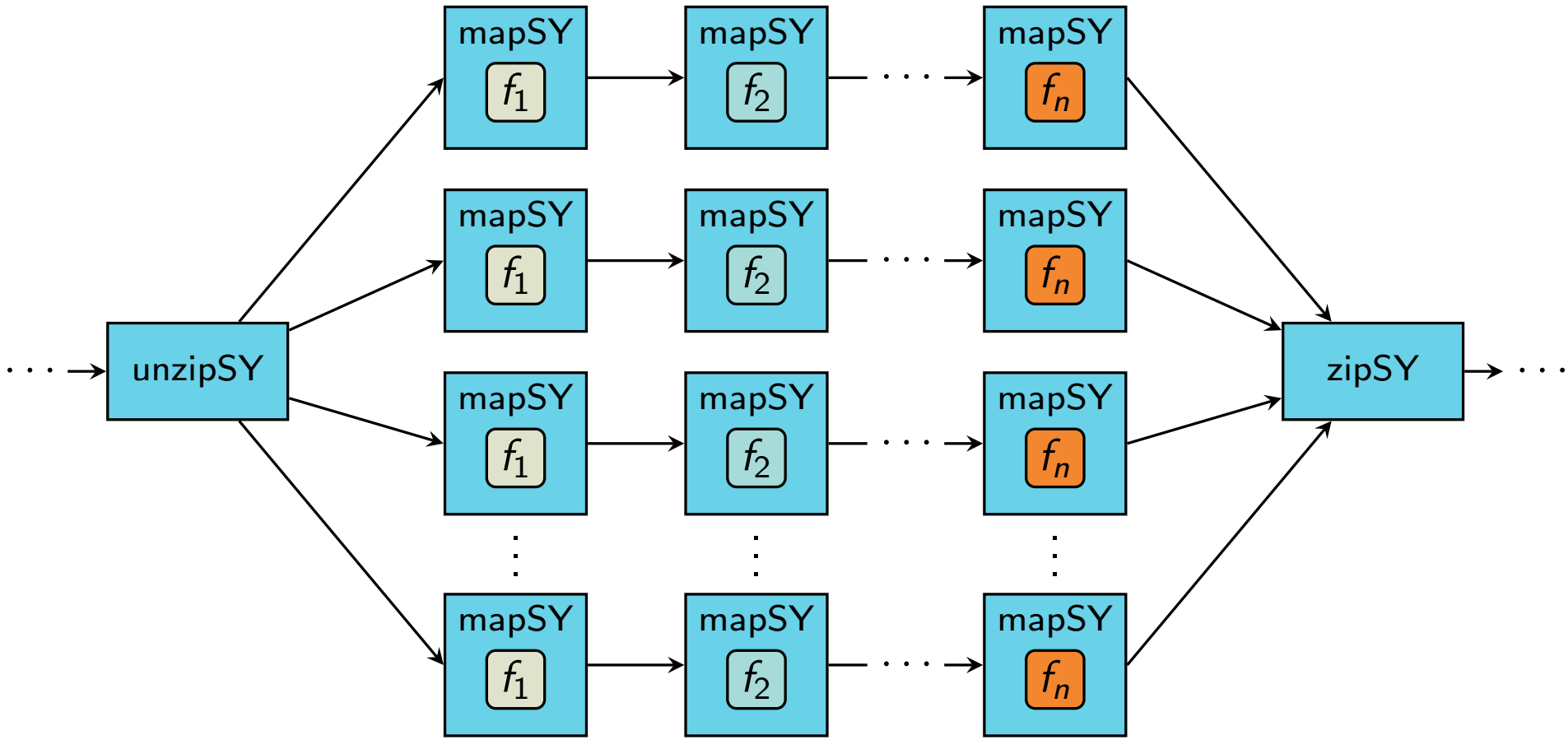
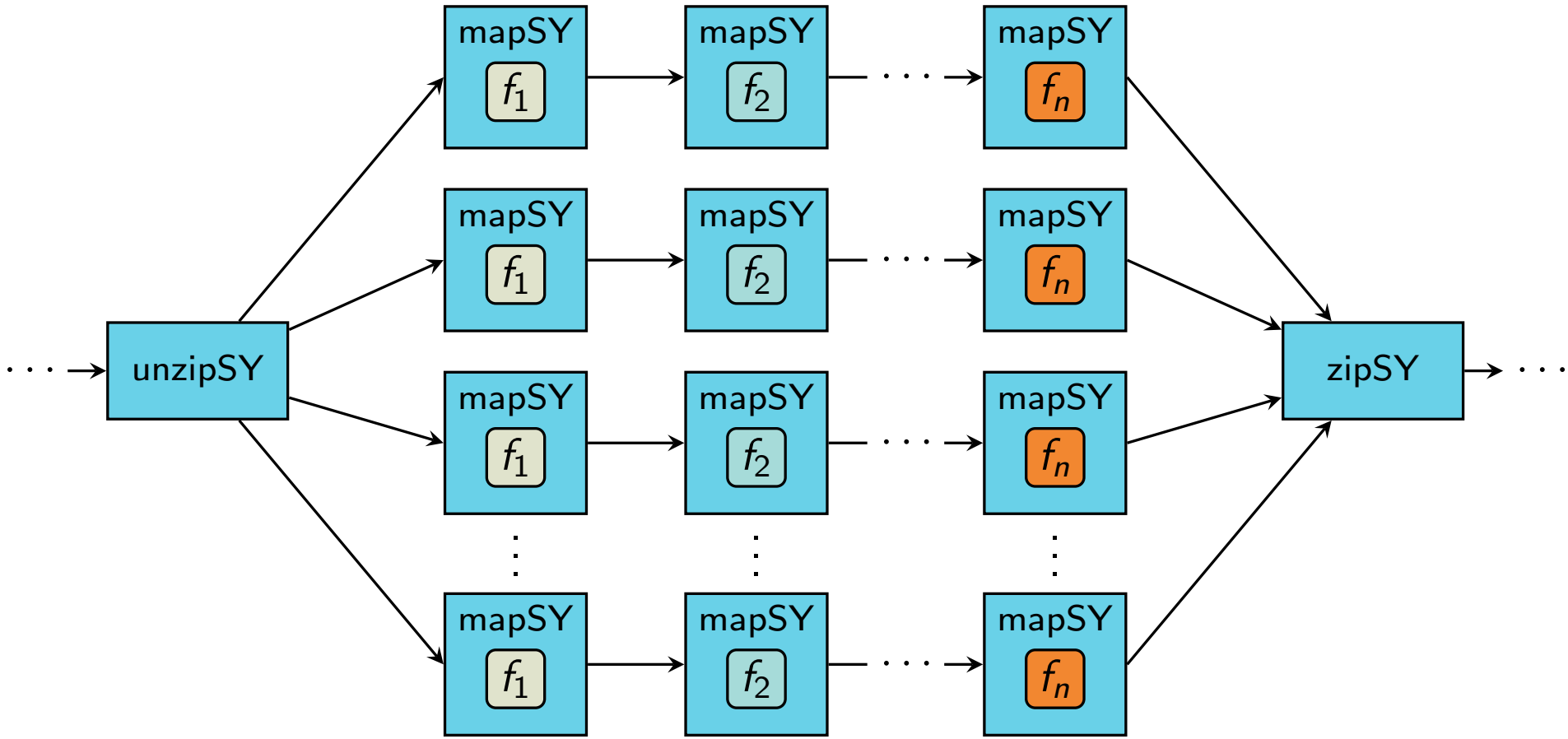
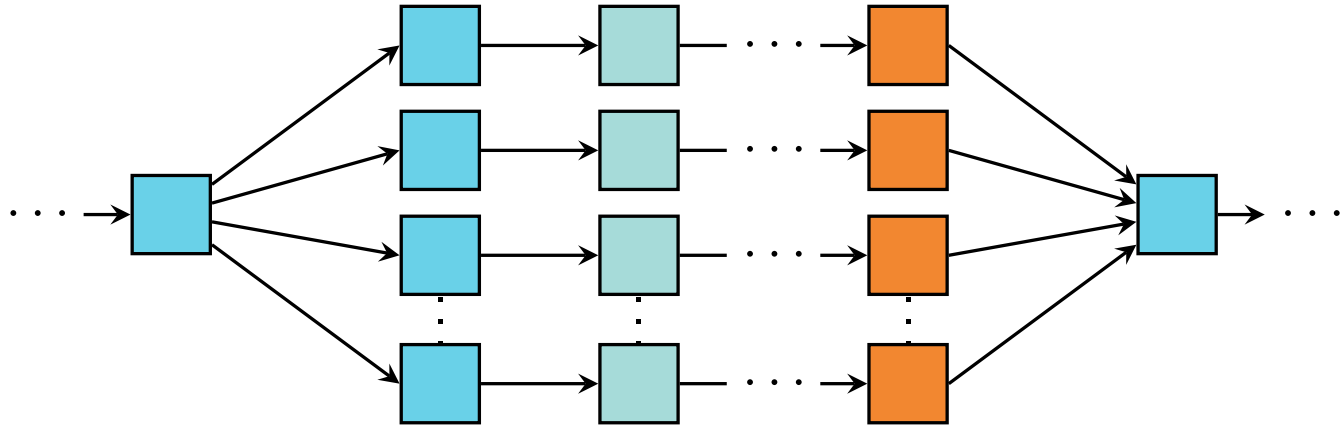


The *split-map-merge* pattern

Want to Handle Only One Function



Method 1: *Section Splitting*



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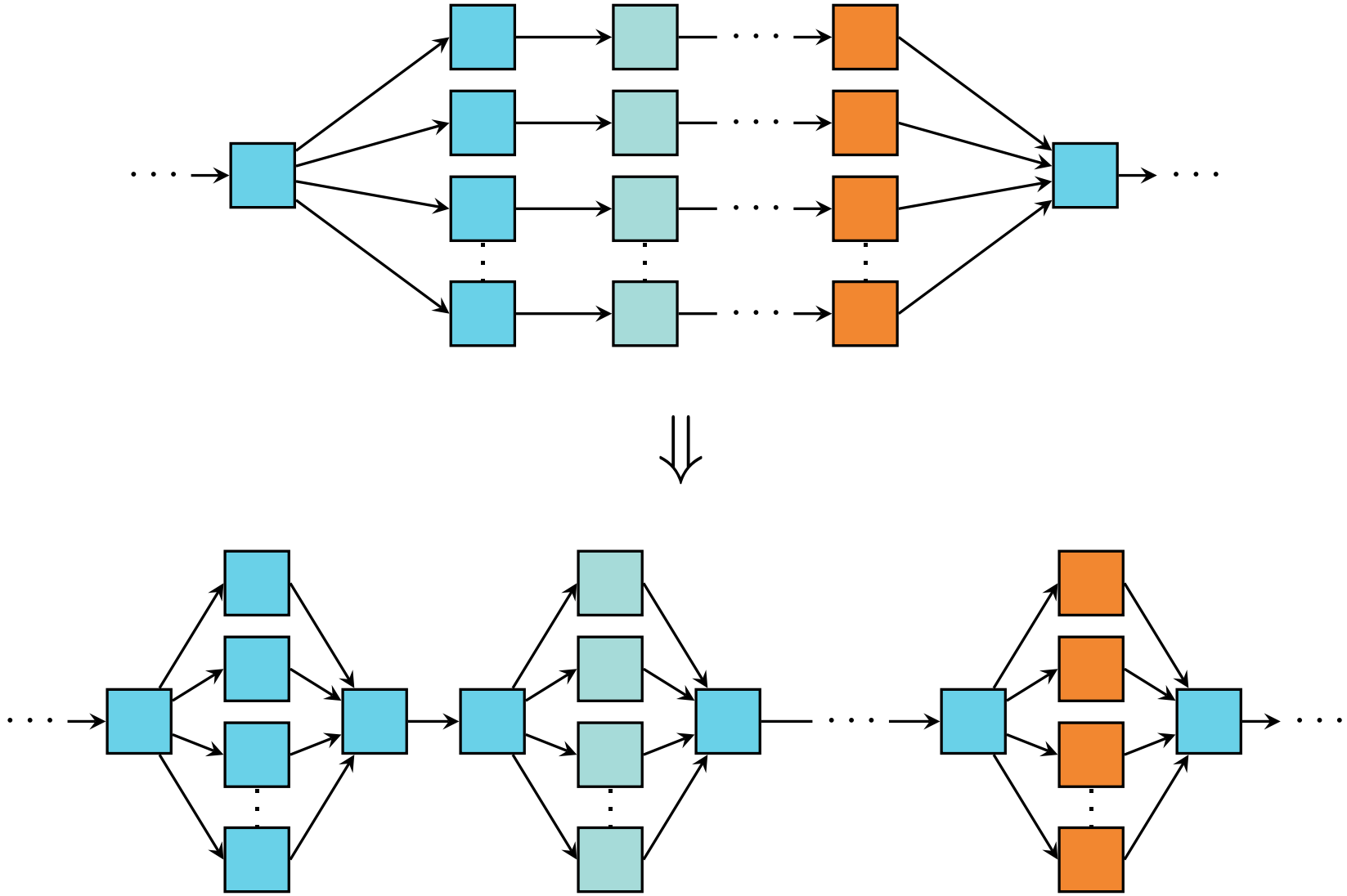
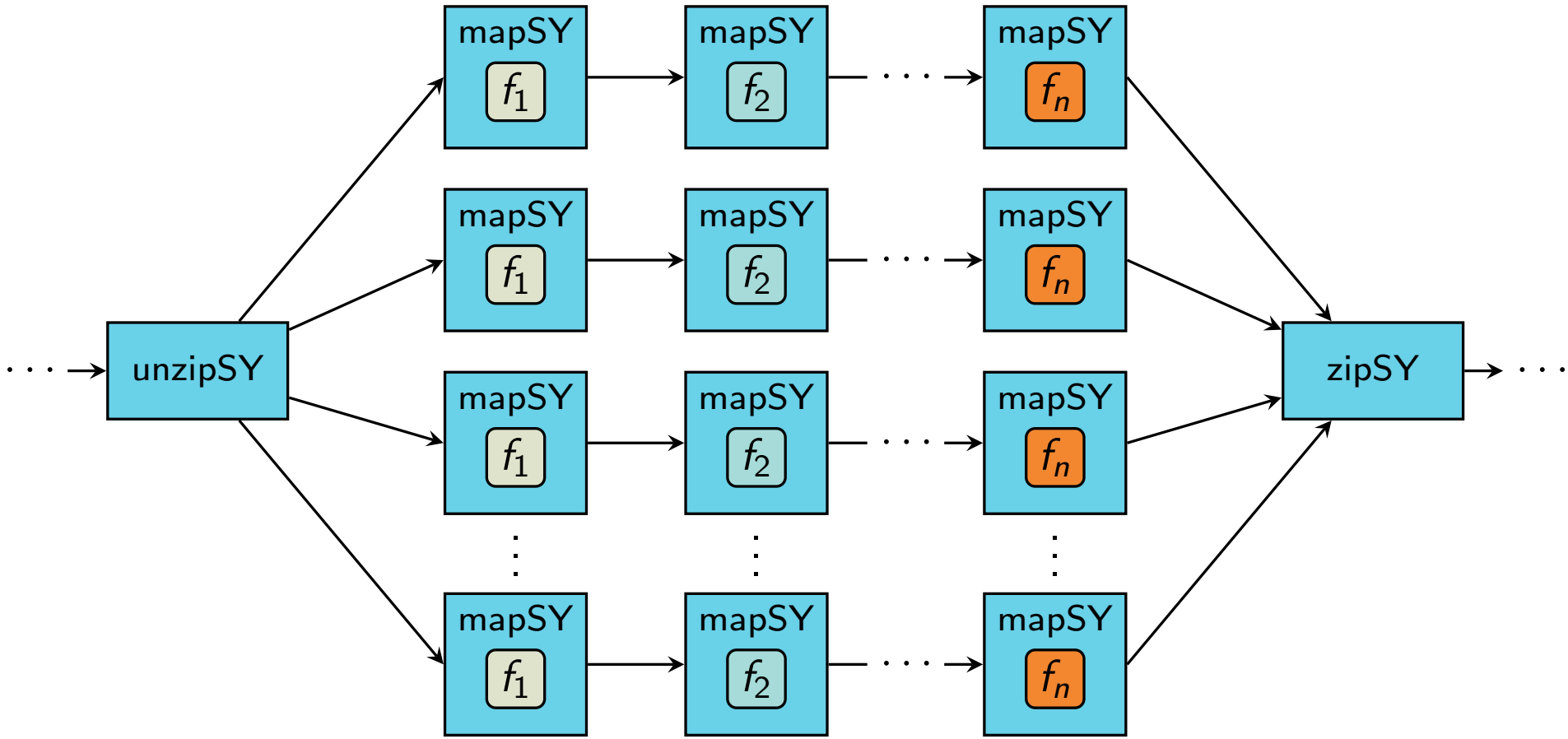


Method 2: *Process Coalescing*



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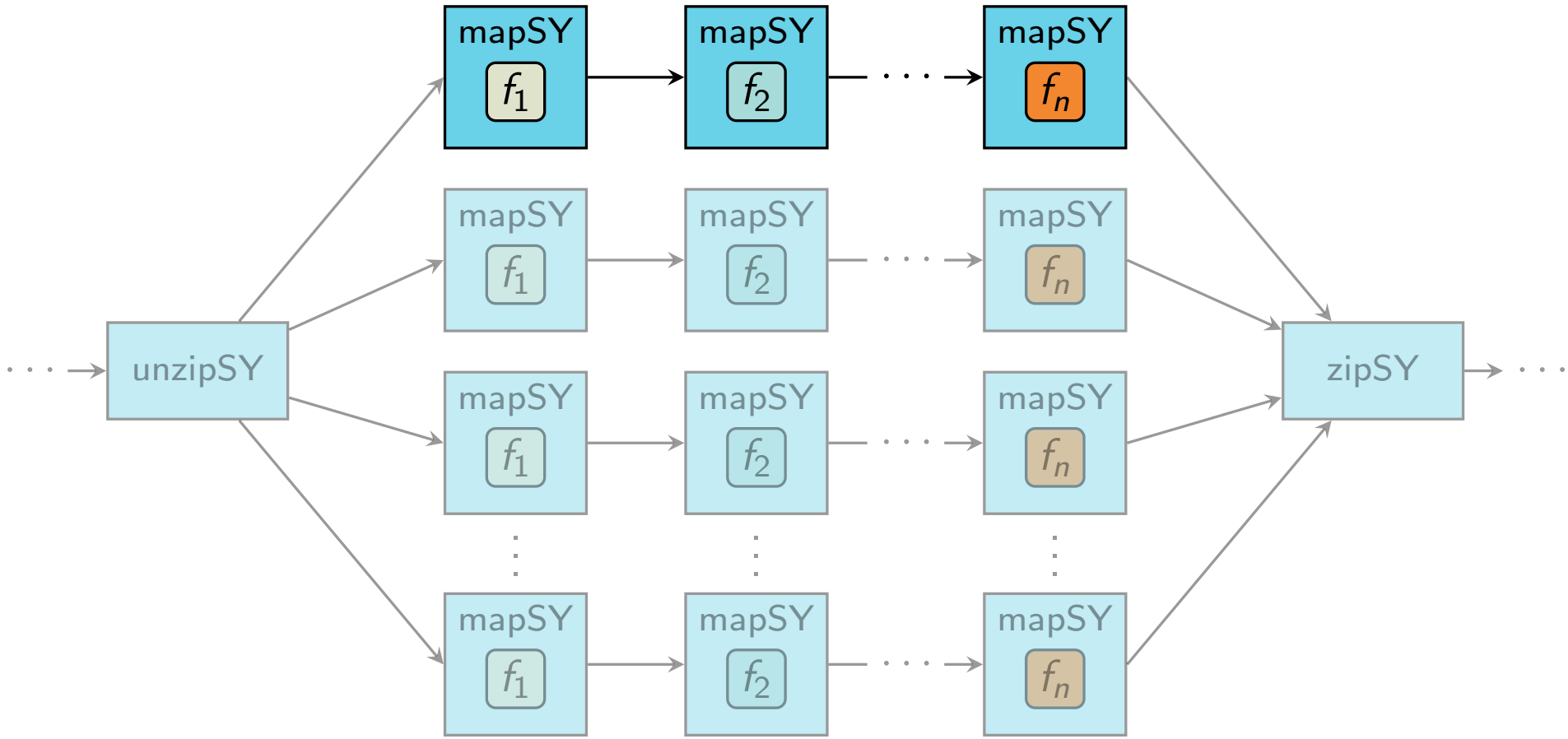

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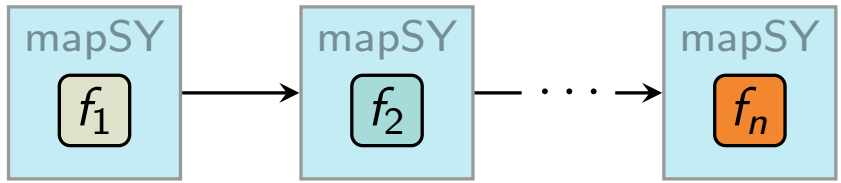

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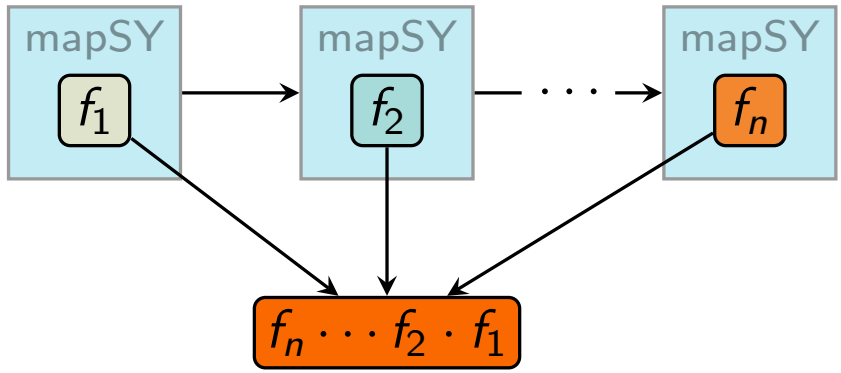

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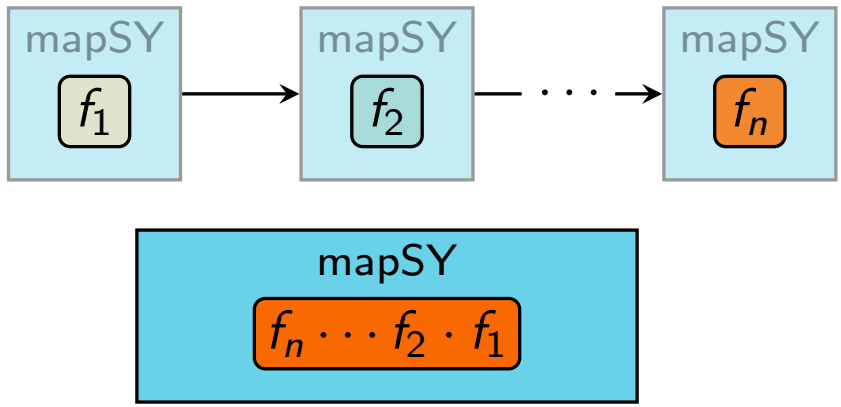

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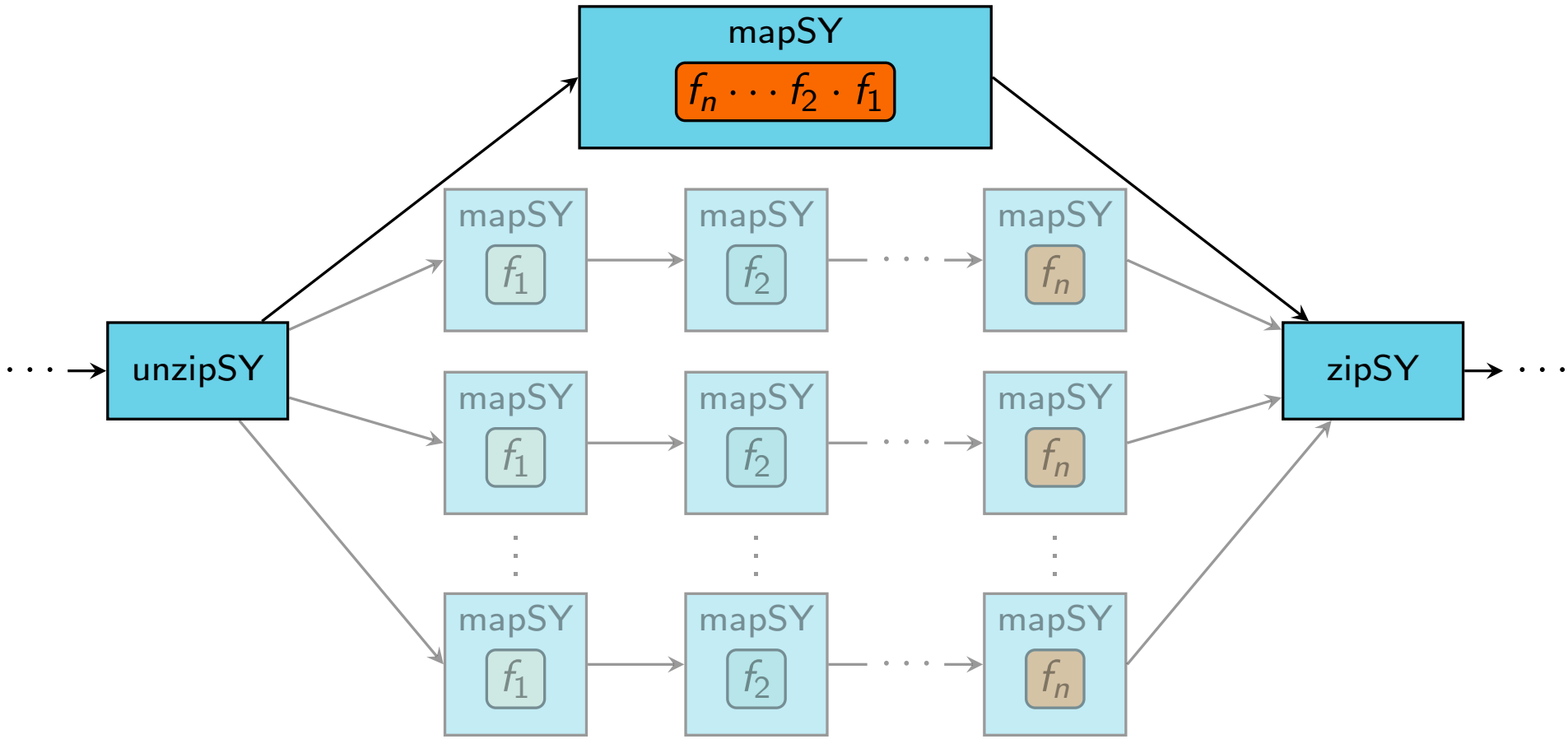

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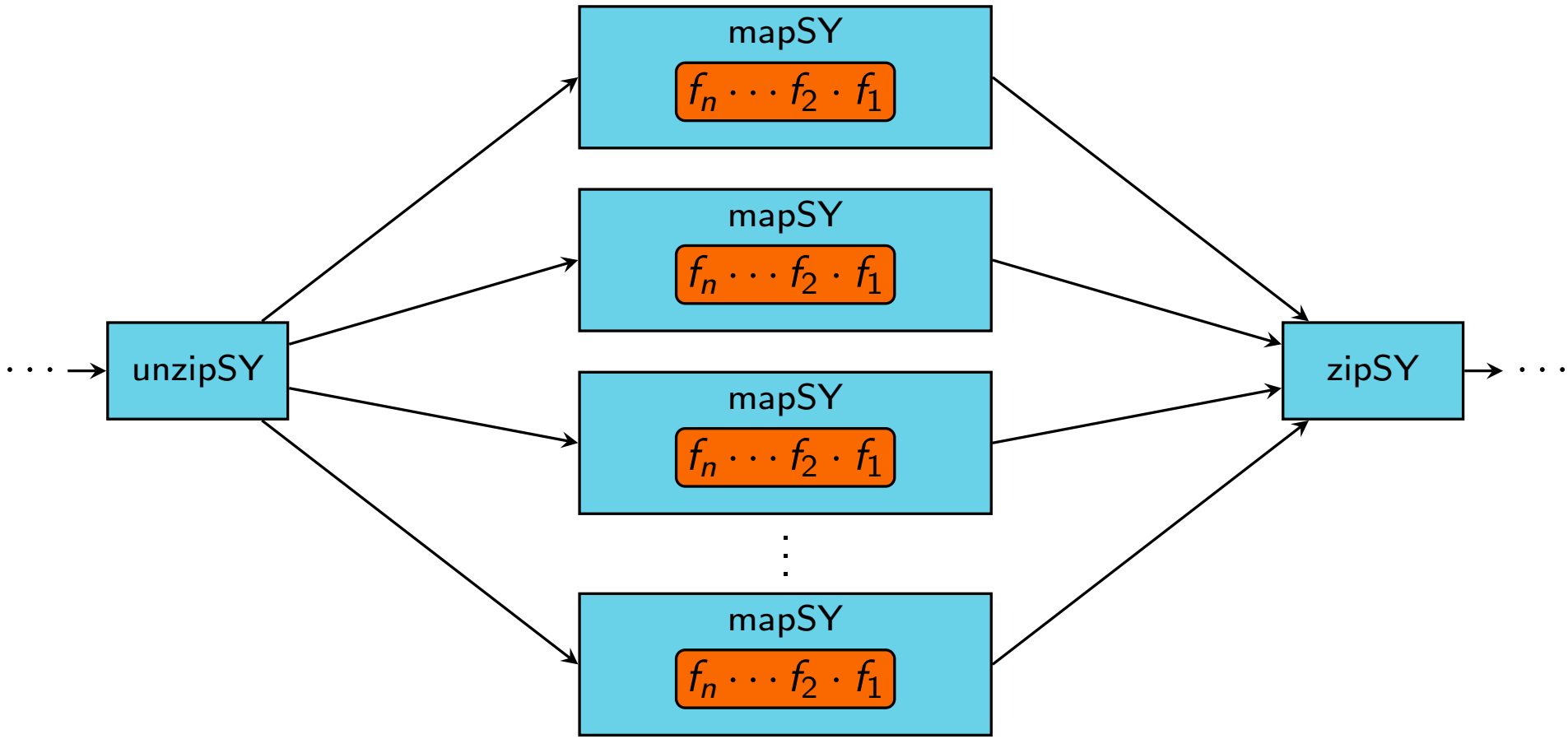
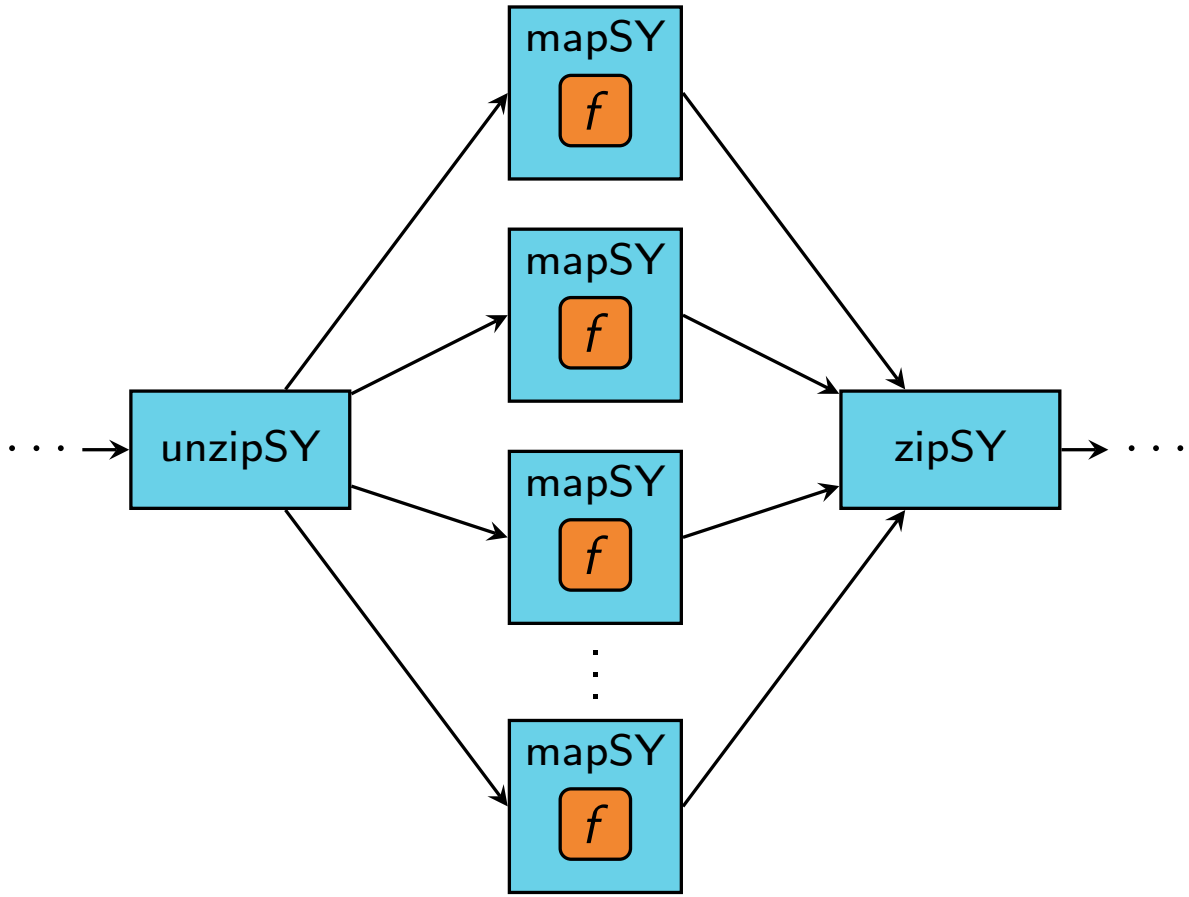
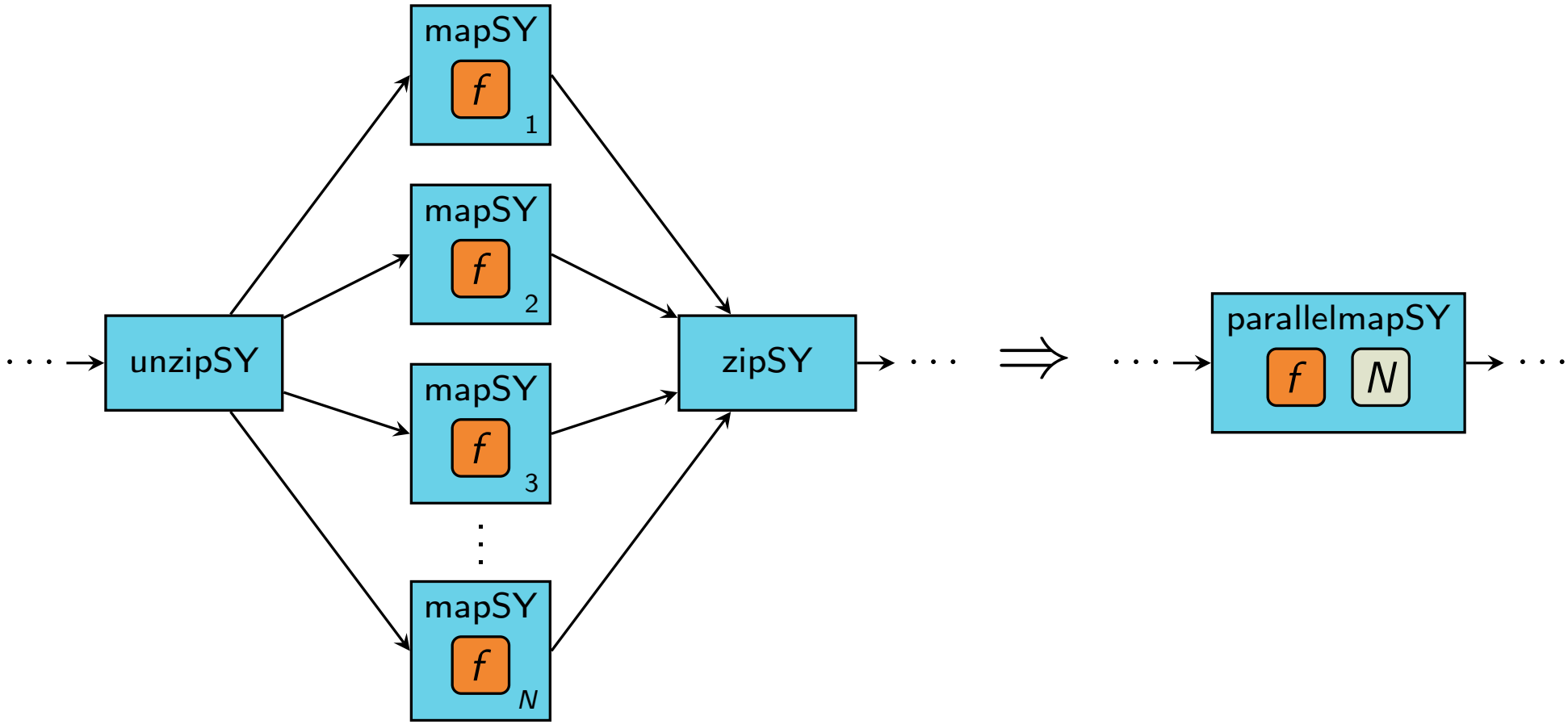


Fuse Zip-Map-Unzip Structures Into *ParallelMaps*



Fuse Zip-Map-Unzip Structures Into *ParallelMaps*



Synthesis

Synthesis

- ParallelmapSY processes:

Synthesis

- ParallelmapSY processes:
  - Choose C or CUDA C implementation

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Synthesis

- ParallelmapSY processes:
  - Choose C or CUDA C implementation
  - Choose to use shared memory in CUDA C implementation
- Other processes:
  - Always C implementation

f2cc

f2cc

- *ForSyDe-2-CUDA C*

f2cc

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- Proof-of-concept synthesis tool

f2cc

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f2cc

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f2cc

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f2cc

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f2cc

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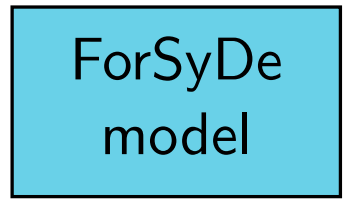

f2cc

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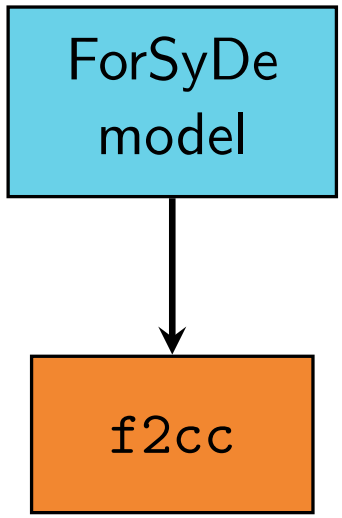

f2cc

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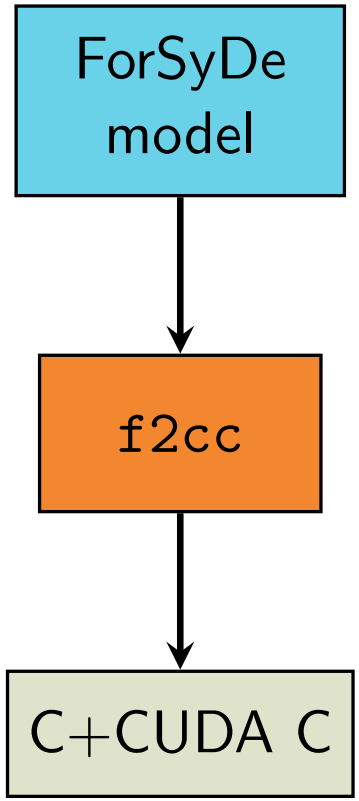

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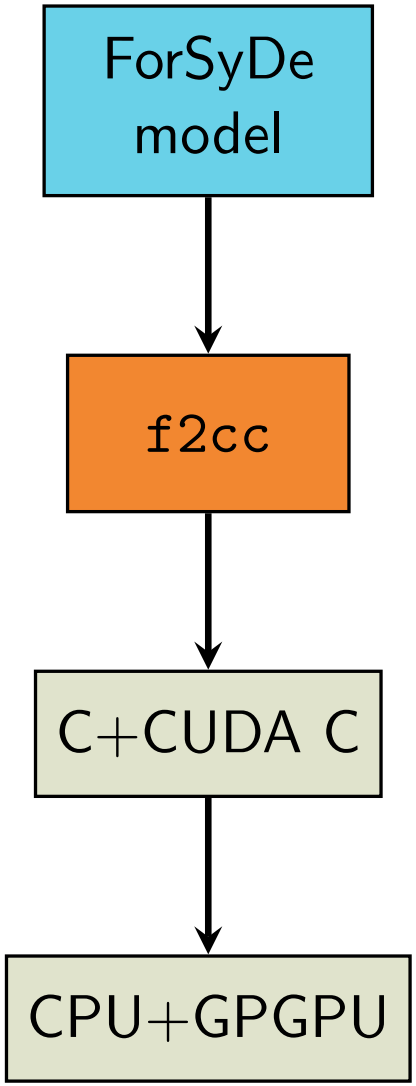

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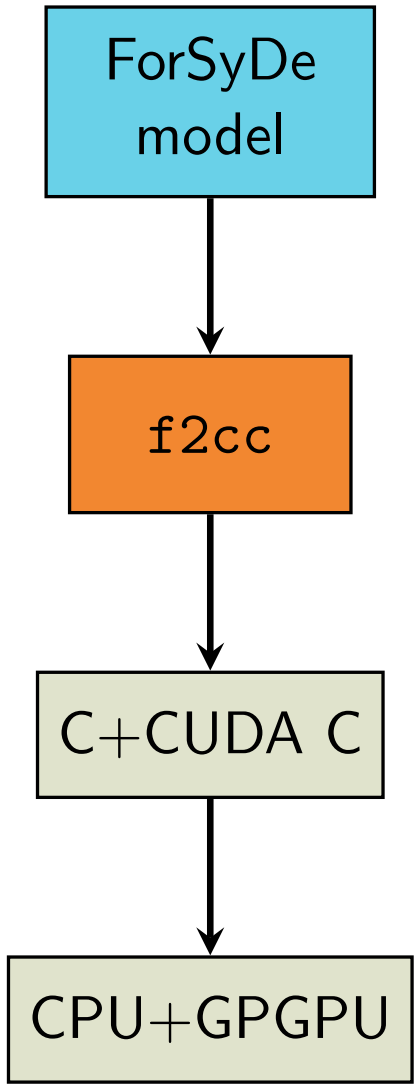

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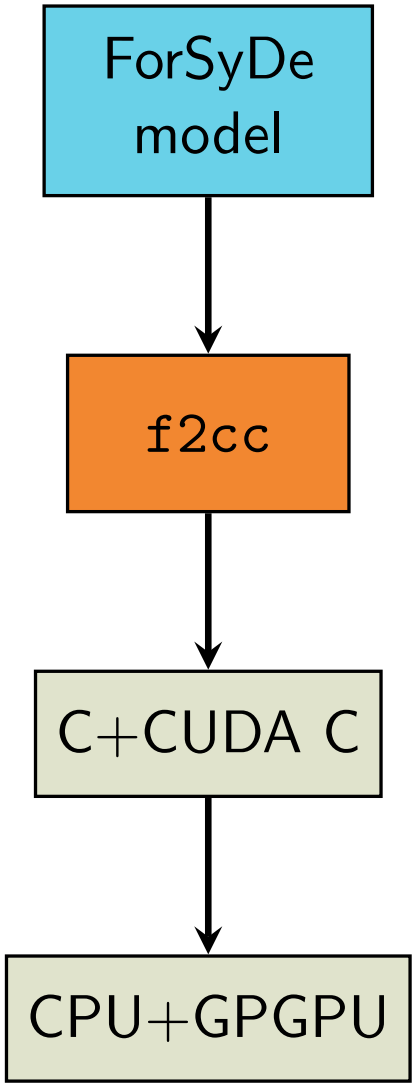

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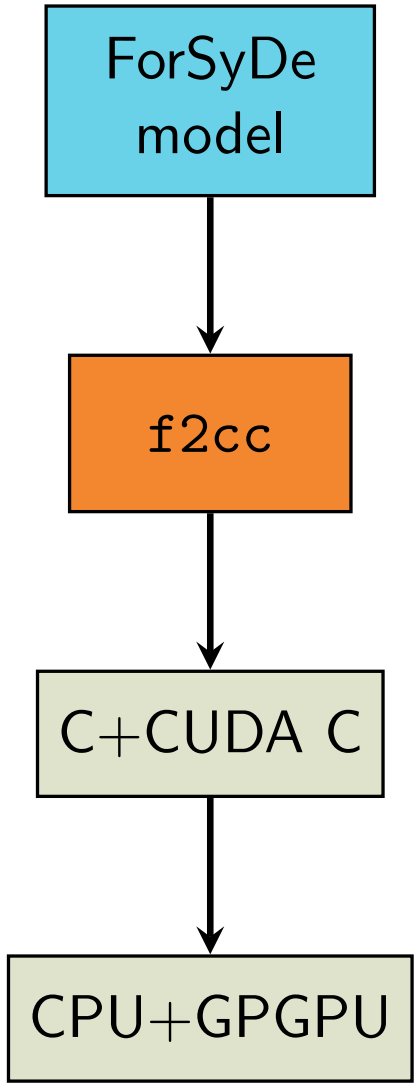

Experiments: Setup and Expectations

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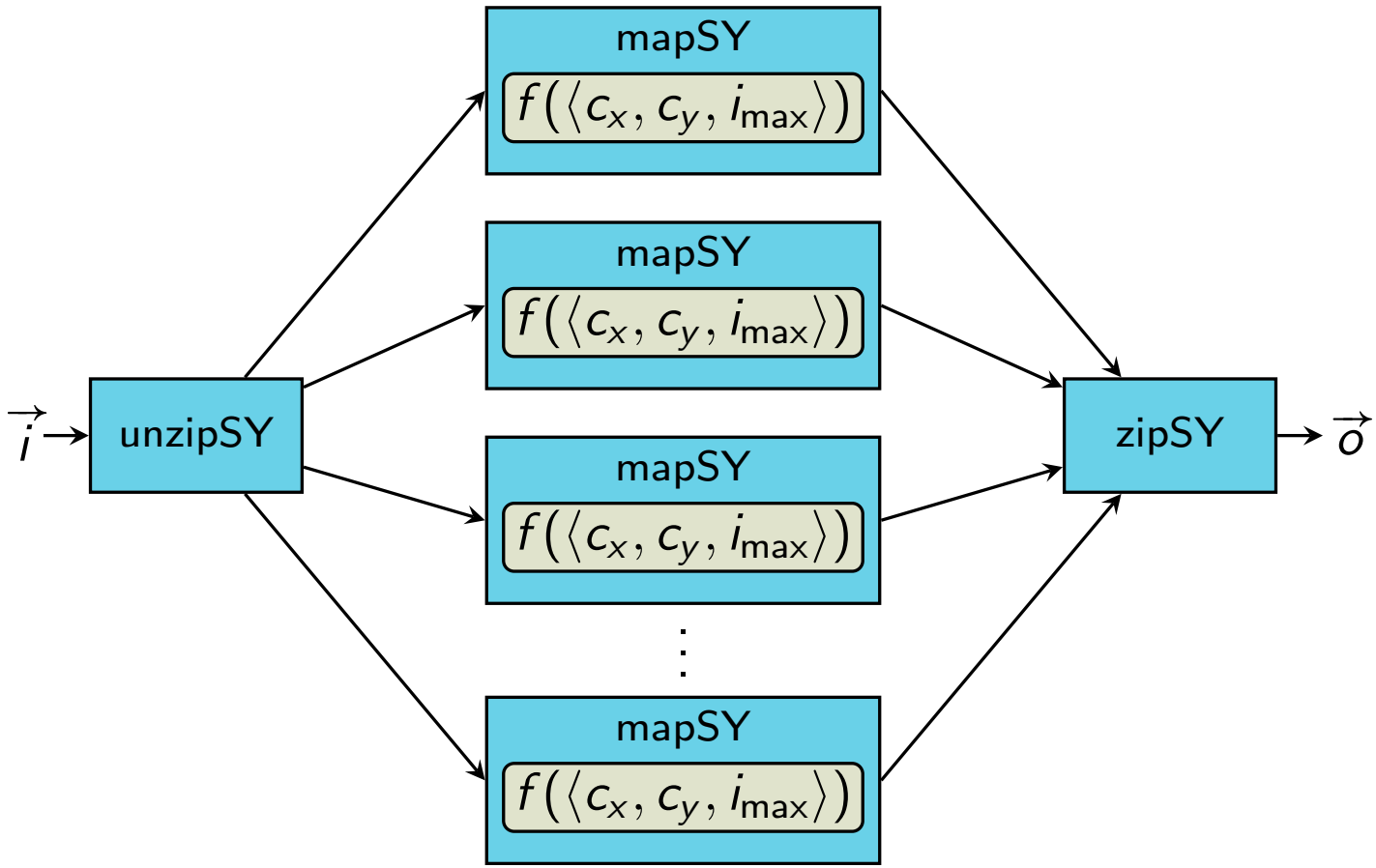
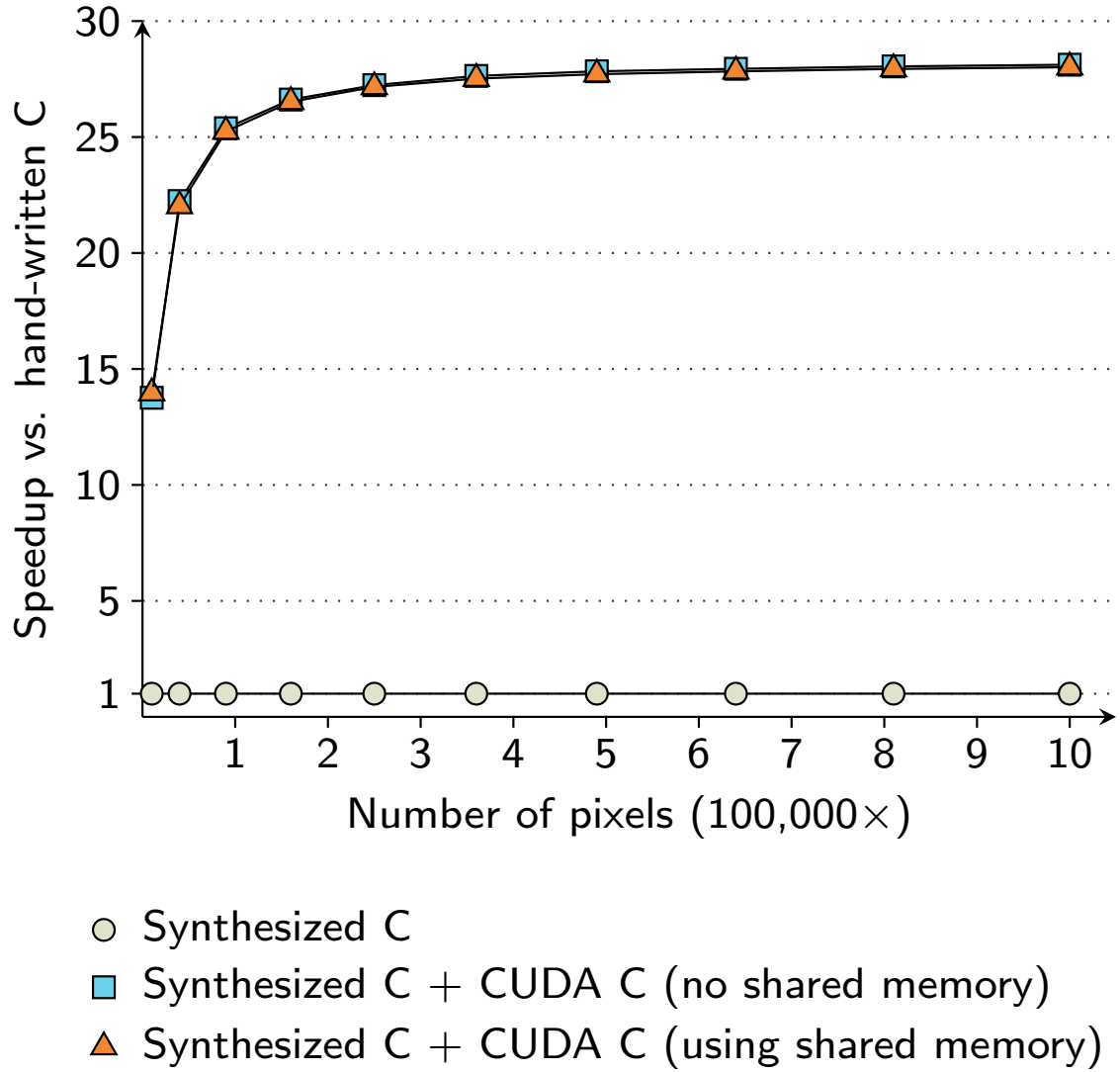
    - $\backsim$ 30$\times$ speedup is good

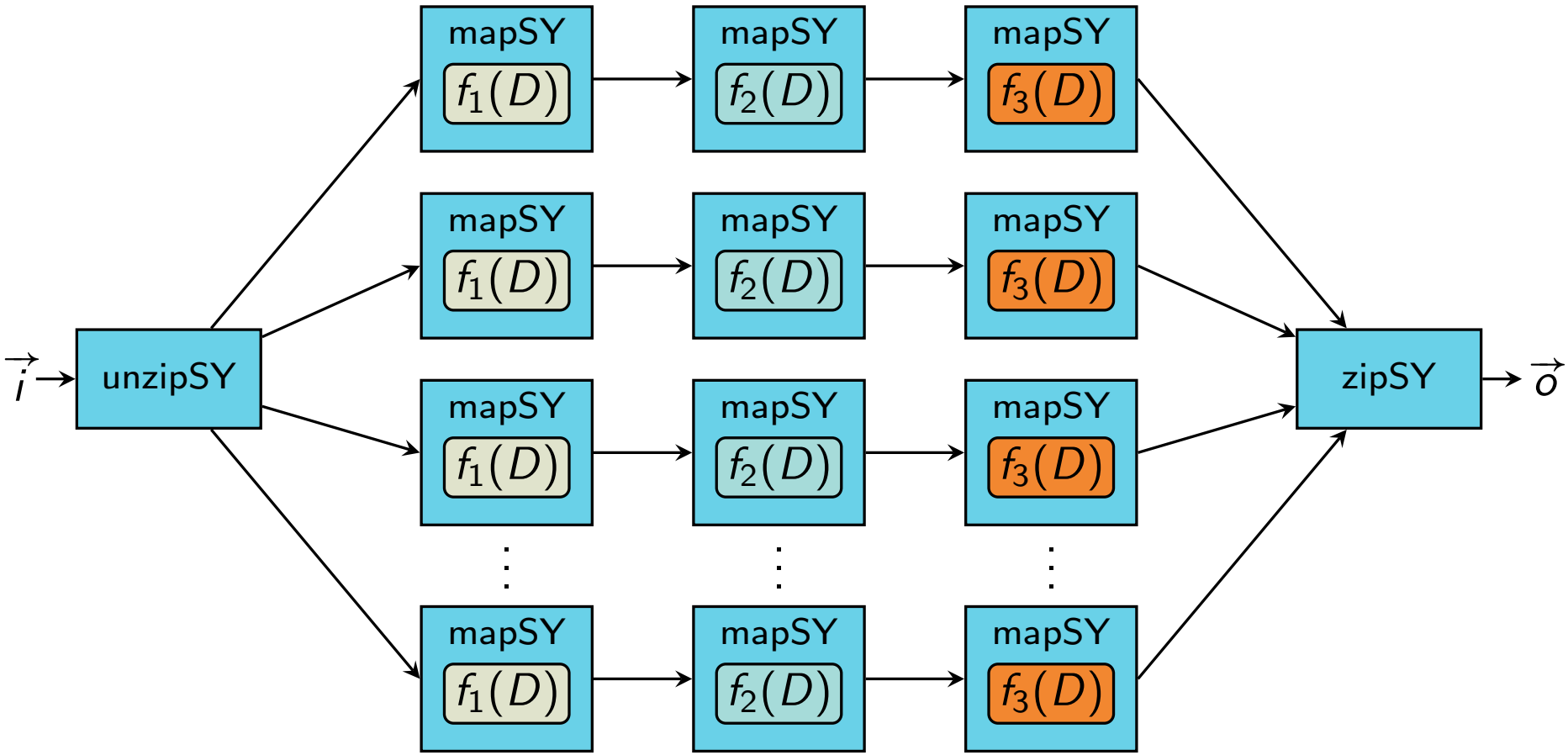
ForSyDe Model of Mandelbrot Application



Achieve Expected Outcome for Mandelbrot Application

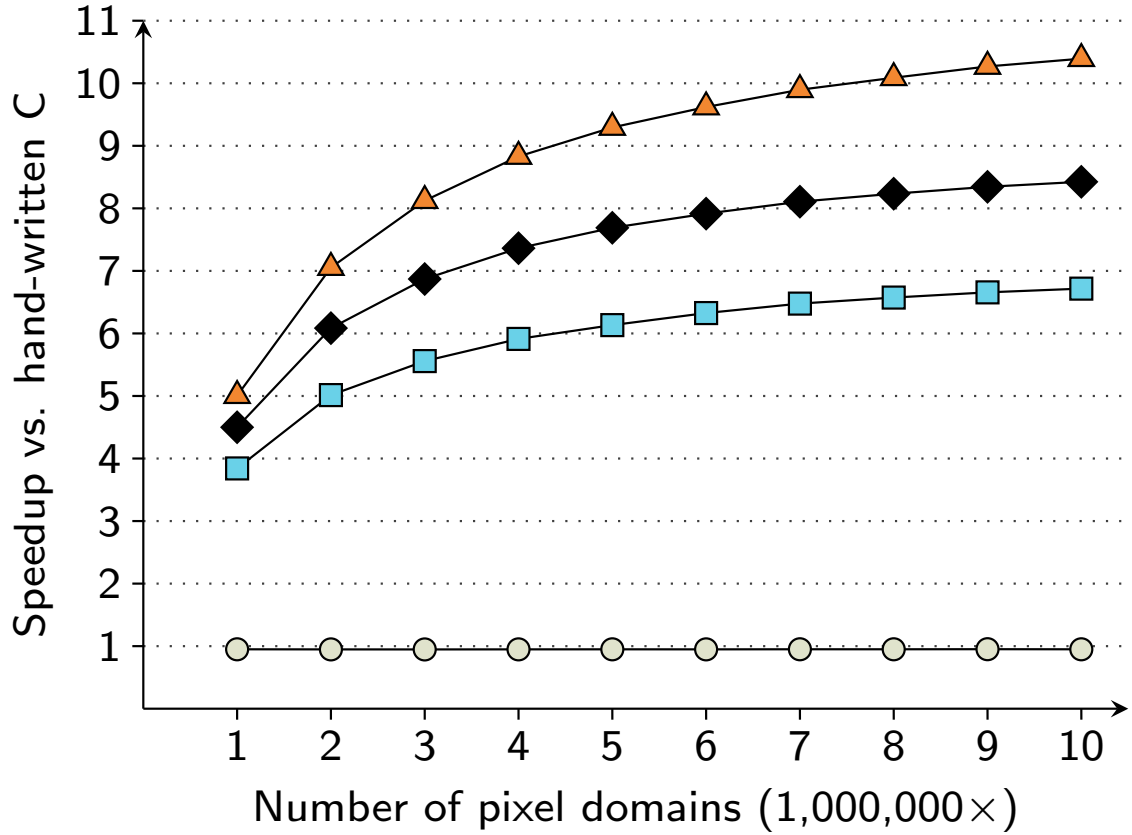


ForSyDe Model of Image Processing Application



$$D = \langle p_1, p_2, p_3, p_4, p_5, p_6, p_7 \rangle$$

Achieve Expected Outcome for Image Processing Application



- Synthesized C
- Synthesized C + CUDA C (section splitting, no shared memory)
- Synthesized C + CUDA C (process coalescing, no shared memory)
- Synthesized C + CUDA C (process coalescing, with shared memory)

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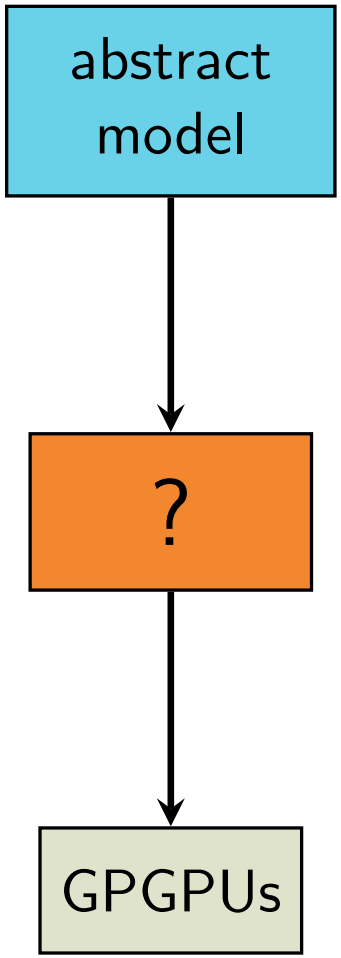
  - Look into DSE (design space exploration)
- Eager memory-copying scheme
  - Reduce overhead through lazy copying

Summary

Summary



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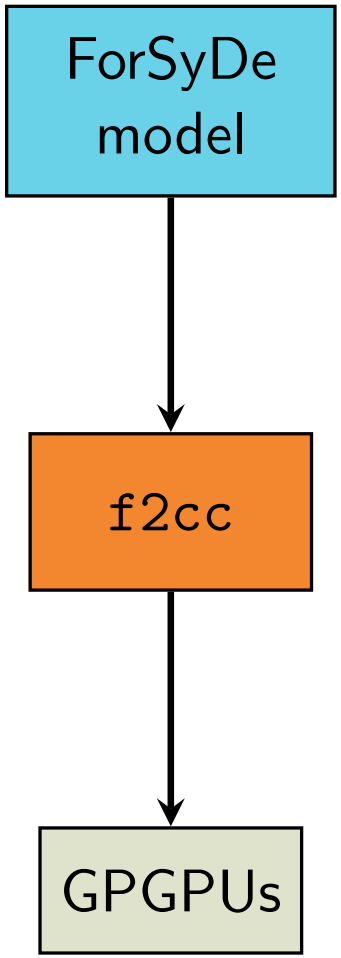

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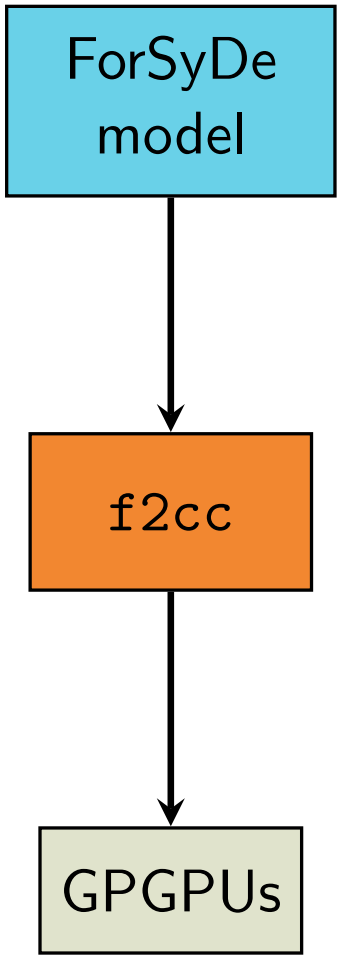

- Get high-performance implementation for supported design pattern

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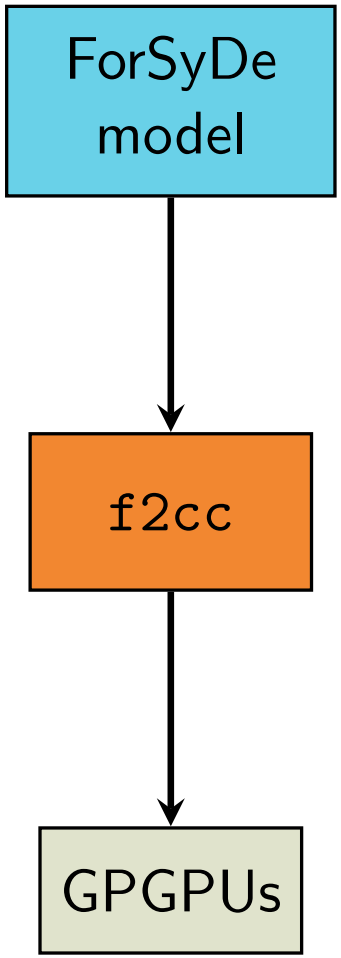
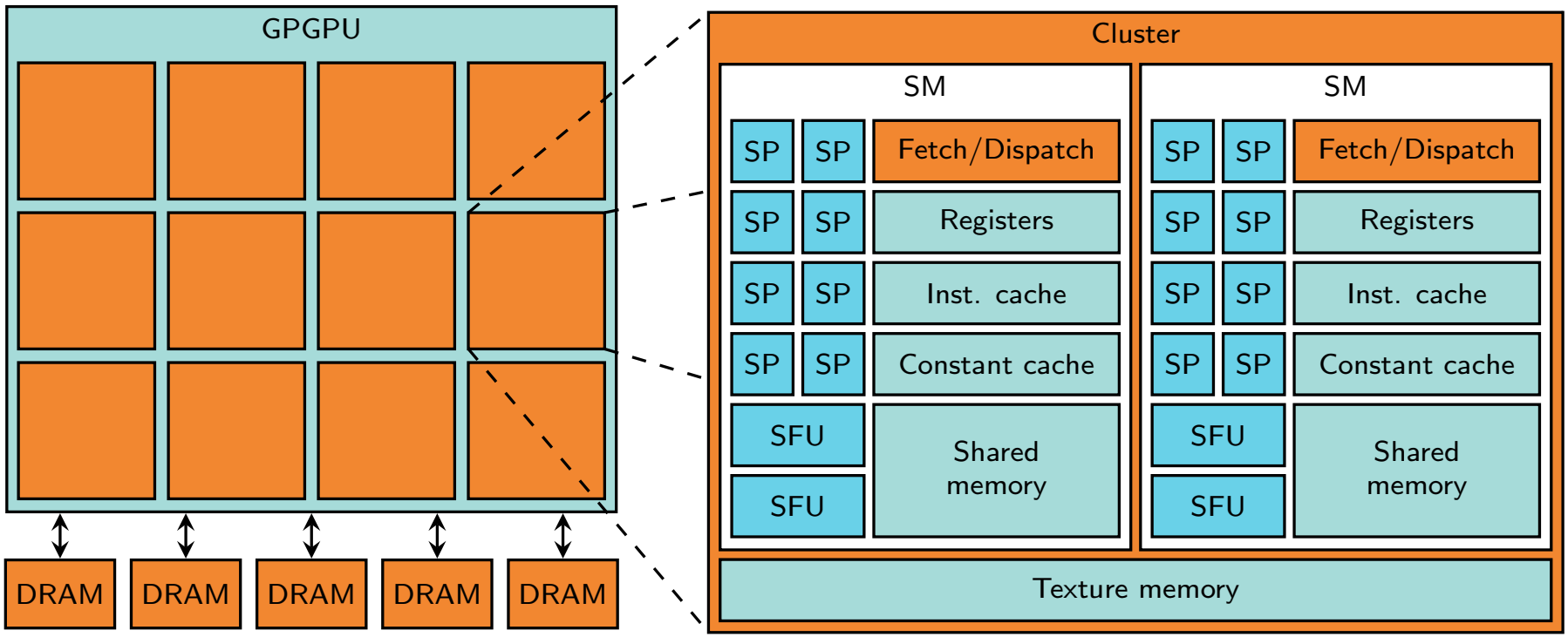


- Get high-performance implementation for supported design pattern

`f2cc` available at:
`https://forsyde.ict.kth.se/trac/wiki/ForSyDe/f2cc`

NVIDIA's GPGPU Architecture



```
<graphml>
  <graph id="test" edgedefault="directed">
    ...
    <node id="unzip"> ... </node>
    <node id="zip"> ... </node>
    <node id="map1">
      <data key="process_type">mapSY</data>
      <data key="procfun_arg">
        int f1(int x) { return x + 1; }
      </data>
      <port name="in" /><port name="out" />
    </node>
    <node id="map6">
      <data key="process_type">mapSY</data>
      <data key="procfun_arg">
        int f2(int x) { return x * 2; }
      </data>
      <port name="in" /><port name="out" />
    </node>
    <edge source="unzip" sourceport="out1" target="map1"
          targetport="in" />
    <edge source="map1" sourceport="out" target="map4"
          targetport="in" />
    ...
  </graph>
</graphml>
```

Function Produced From Process Coalescing

```
__device__
int f12(int x) {
    int res_f1 = f1(x);
    int res_f2 = f2(res_f1);
    return res_f2;
}
```

Kernel Function Produced (Without Shared Memory)

```
__global__
void f12_kernel(
  const int* input,
  int* output,
  int offset)
{
  unsigned int global_index =
    (blockIdx.x * blockDim.x + threadIdx.x) + offset;

  if (global_index < 3) {
    int input_index = global_index * 1;


    output[global_index] = f12(input[input_index]);
  }
}
```

Kernel Function Produced (With Shared Memory)

```
__global__
void f12_kernel(
  const int* input,
  int* output,
  int offset)
{
  unsigned int global_index =
    (blockIdx.x * blockDim.x + threadIdx.x) + offset;
  extern __shared__ int input_cached[];
  if (global_index < 3) {
    int input_index = threadIdx.x * 1;
    int gi_index = global_index * 1;
    input_cached[input_index + 0] = input[gi_index + 0];
    output[global_index] = f12(input_cached[input_index]);
  }
}
```

Produced Invoker Function (1 of 3)

```
void f12_invoker(const int* input, int* output) {
  int* device_input;
  int* device_output;

  struct cudaDeviceProp prop;
  cudaGetDeviceProperties(&prop, 0);

  int tlimit = prop.maxThreadsPerBlock *
               prop.multiProcessorCount;

  cudaMalloc((void**) &device_input, 3 * sizeof(int));
  cudaMalloc((void**) &device_output, 3 * sizeof(int));
  cudaMemcpy((void*) device_input,
             (void*) input,
             3 * sizeof(int),
             cudaMemcpyHostToDevice);
```

Produced Invoker Function (2 of 3)

```
if (prop.kernelExecTimeoutEnabled) {
  int num_t_left = 3;
  int offset = 0;
  while (num_t_left > 0) {
    int num_t_exec =
      num_t_left < tlimit ? num_t_left : tlimit;
    KernelConfig c = calculateBestKernelConfig(...);
    f12_kernel<<<c.grid, c.threadBlock, c.sharedMemory>>>
      (device_input, device_output, offset);
    int num_t_exed = c.grid.x * c.threadBlock.x;
    num_t_left -= num_t_exed;
    offset += num_t_exed;
  }
}
else {
  KernelConfig c = calculateBestKernelConfig(...);
  f12_kernel<<<c.grid, c.threadBlock, c.sharedMemory>>>
    (device_input, device_output, 0);
}
```

Produced Invoker Function (3 of 3)

```
  cudaMemcpy((void*) output,
             (void*) device_output,
             3 * sizeof(int),
             cudaMemcpyDeviceToHost);
  cudaFree((void*) device_input);
  cudaFree((void*) device_output);
}
```