Constraint-Based Code Generation

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Outline

1. Background & Motivation
2. Our Approach
3. Instruction Selection
4. Instruction Scheduling
5. Register Allocation
6. Challenges and Future Work

1 Background & Motivation

2 Our Approach

3 Instruction Selection

4 Instruction Scheduling

5 Register Allocation

6 Challenges and Future Work

What is code generation?

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- Target-independent program representation $\rightarrow$ Optimized target-specific assembly code

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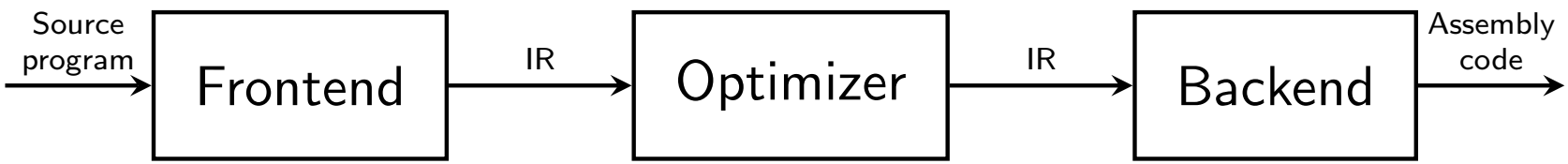
- Target-independent program representation $\rightarrow$ Optimized target-specific assembly code
  - One of the oldest computer science problems
- Set of interdependent NP-complete problems
  - Traditionally solved using non-optimal heuristics
  - Phase ordering

Traditional compiler

Traditional compiler



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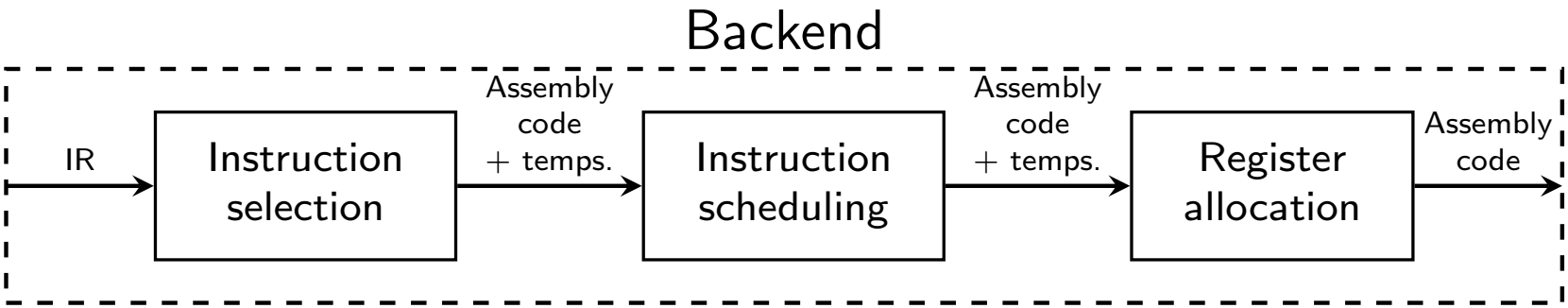

Intermediate representation (IR)

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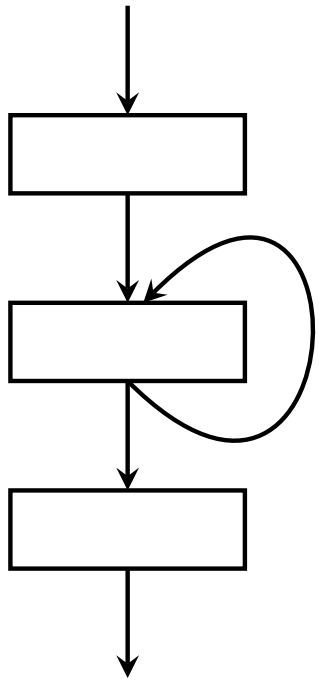
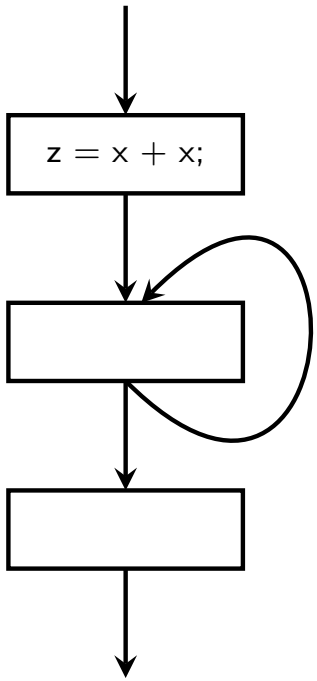


Control flow graph
(CFG), per function

Intermediate representation (IR)



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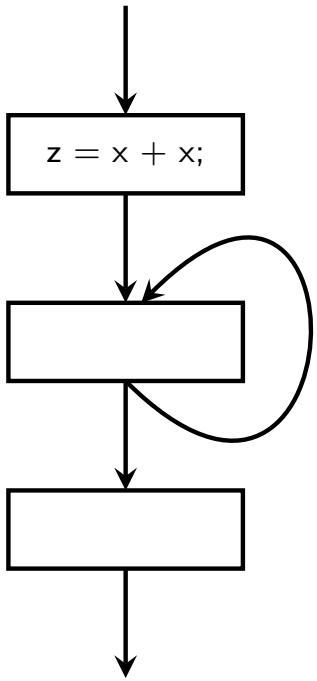

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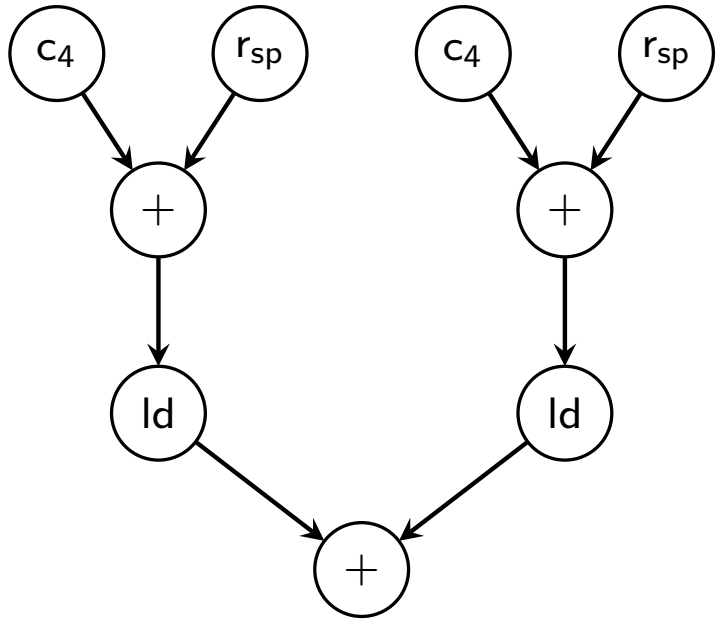
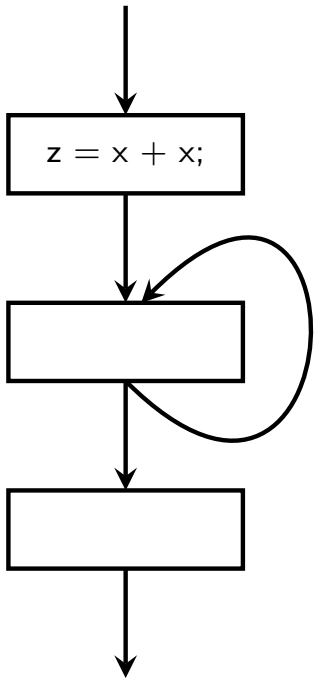


Expression tree, per block

Intermediate representation (IR)



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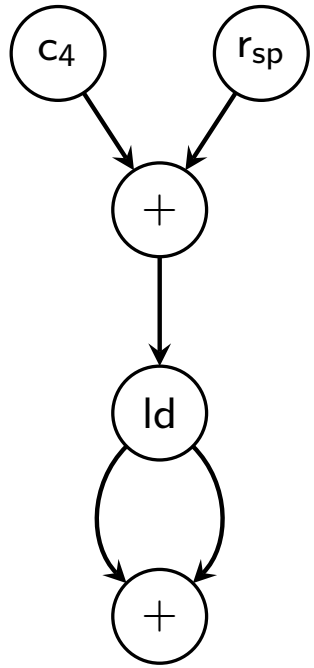
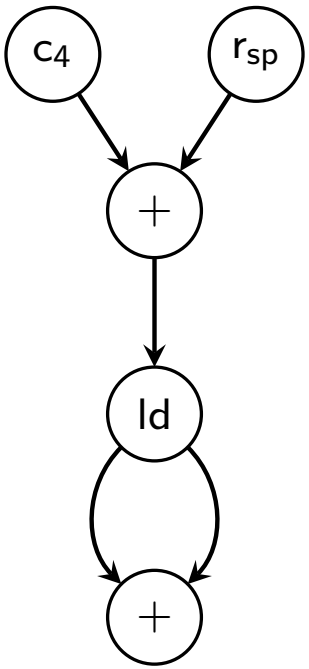


Directed acyclic graph (DAG)

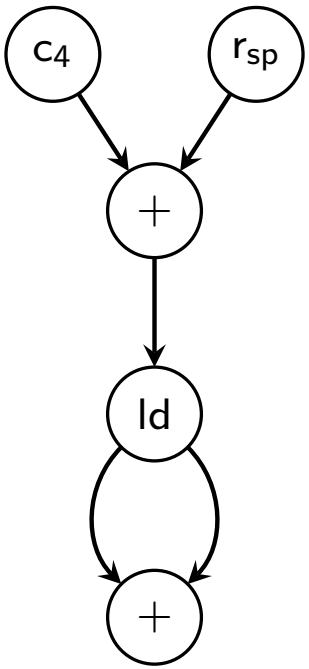
From DAGs to assembly code

From DAGs to assembly code



From DAGs to assembly code

- Select which CPU instructions to use



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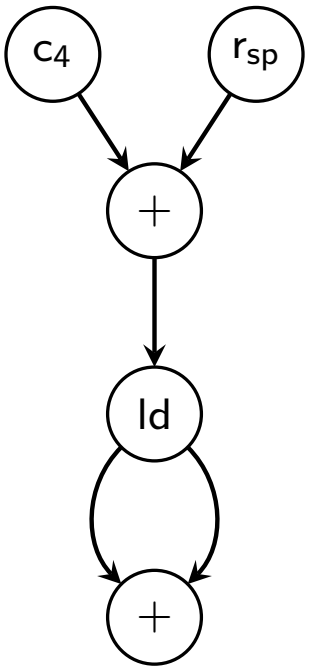

- Select which CPU instructions to use
  - Find covering with least cost

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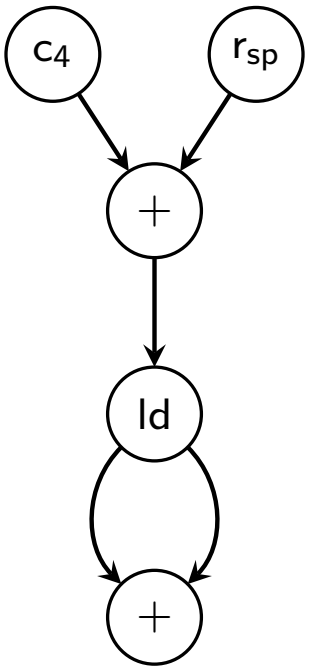

- Select which CPU instructions to use
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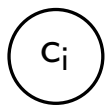
$c = 0$

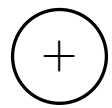
P_1



$c = 1$

`mvi` r, c_i

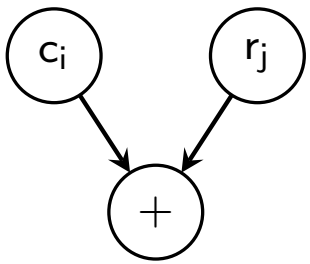
P_2



$c = 1$

`add` r_3, r_1, r_2

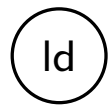
P_3



$c = 1$

`addi` r_d, r_j, c_i

P_4

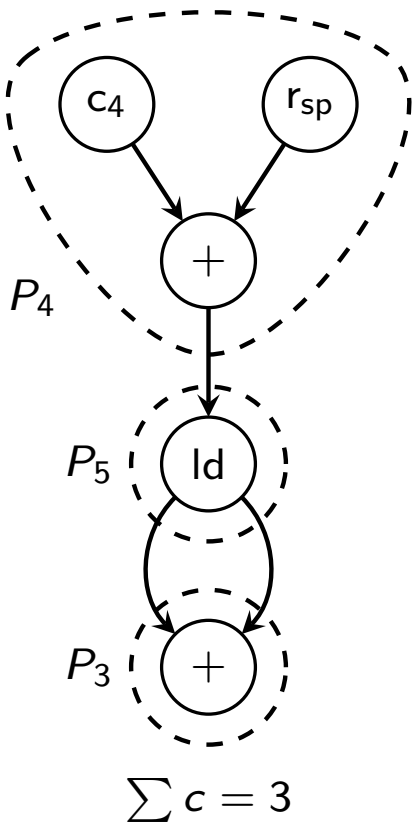


$c = 1$

`ld` r_d, r_{addr}

P_5

From DAGs to assembly code



- Select which CPU instructions to use
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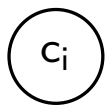
$c = 0$

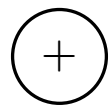
P_1



$c = 1$

`mvi` r, c_i

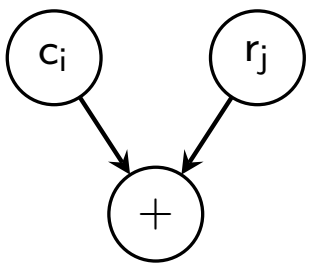
P_2



$c = 1$

`add` r_3, r_1, r_2

P_3



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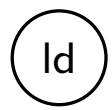
`addi` r_d, r_j, c_i

P_4



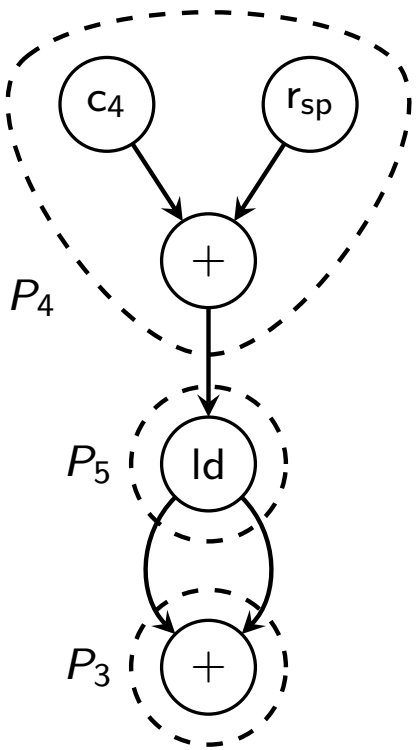
$c = 1$

`ld` r_d, r_{addr}

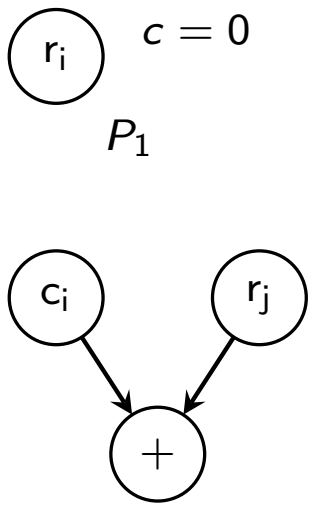
P_5

From DAGs to assembly code

- Select which CPU instructions to use
  - Find covering with least cost



$\sum c = 3$



$\Longrightarrow$

```
addi t0, rsp, 4
ld t1, t0
add tz, t1, t1
```

From DAGs to assembly code

```
addi t0, r_sp, 4
ld t1, t0
add t_z, t1, t1
```

From DAGs to assembly code

```
addi t0, r_sp, 4
ld t1, t0
add t_z, t1, t1
```

- Schedule instructions

From DAGs to assembly code

```
addi t0, r_sp, 4
ld t1, t0
add t_z, t1, t1
```

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

From DAGs to assembly code

```
addi t0, rsp, 4
ld t1, t0
add tz, t1, t1
```

```
addi r0, rsp, 4
ld r1, r0
add r2, r1, r1
```

Requires 3 registers

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

From DAGs to assembly code

```
addi t0, rsp, 4
ld t1, t0
add tz, t1, t1
```

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

```
addi r0, rsp, 4
ld r1, r0
add r2, r1, r1
```

Requires 3 registers

```
addi r0, rsp, 4
ld r0, r0
add r0, r0, r0
```

Requires only 1 register

1 Background & Motivation

2 Our Approach

3 Instruction Selection

4 Instruction Scheduling

5 Register Allocation

6 Challenges and Future Work

Our Approach

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- Constraint programming

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  - Optimality

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*Given enough patience and money to burn while waiting

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  - Instruction selection - concepts / ideas

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Our Approach

- Constraint programming
  - Optimality*
  - Flexible model
  - Integration
- Current status
  - Instruction selection - concepts / ideas
  - Instruction scheduling & register allocation - prototype + paper*

*Given enough patience and money to burn while waiting

*_Constraint-based register allocation and instruction scheduling._ CP2012.

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Instruction Selection

Which DAG node do we cover by which pattern?

Instruction Selection

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1. Identify potential use of patterns in the DAG

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2. Find optimal covering

Instruction Selection

1. Identify potential use of patterns in the DAG
   - Use existing $O(n)$ techniques
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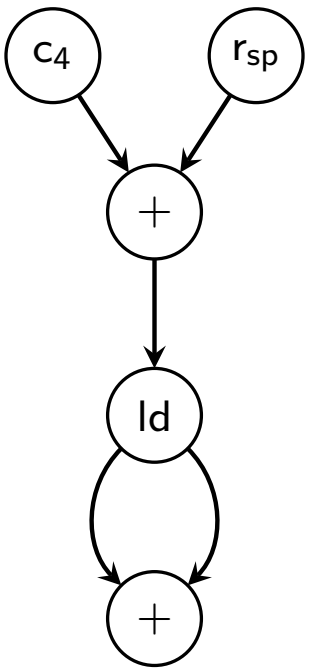
Instruction Selection

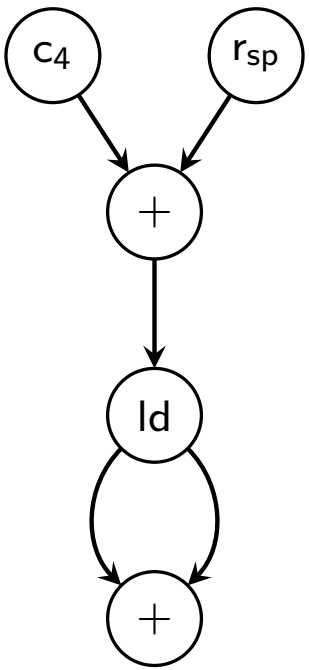
1. Identify potential use of patterns in the DAG
   - Use existing $O(n)$ techniques
2. Find optimal covering
   - Build and solve a constraint model

Instruction Selection



Instruction Selection

- Variables:



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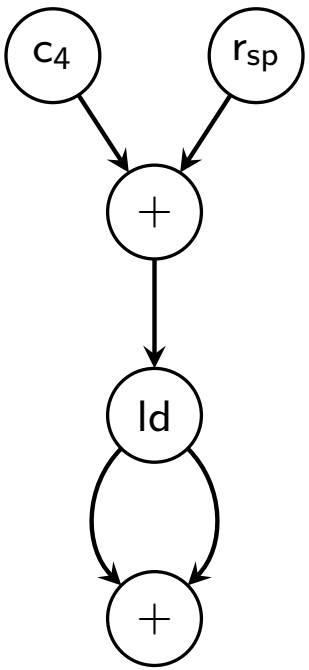
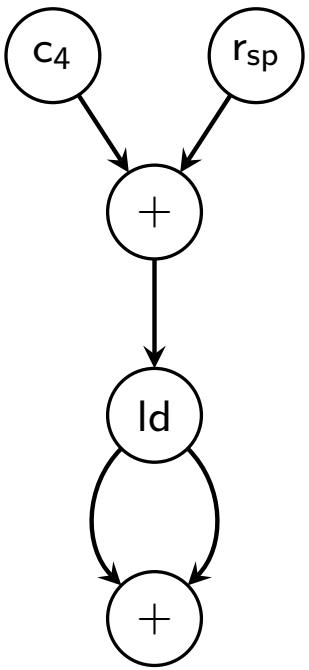


- Variables:
  - One integer variable for each DAG node to decide by which pattern instance is it covered

Instruction Selection



- Variables:
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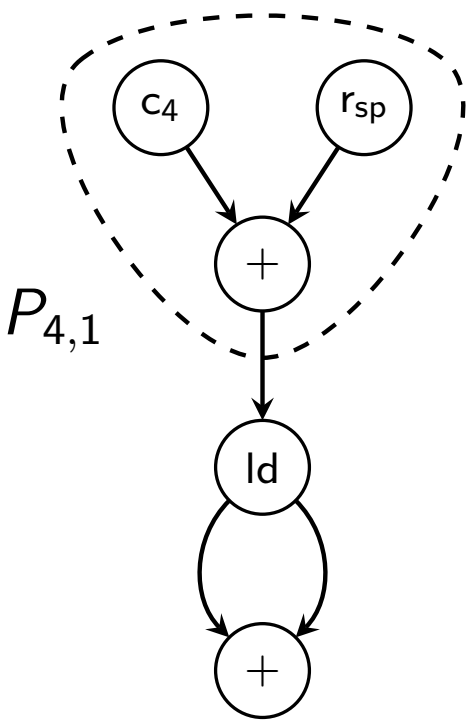
Instruction Selection



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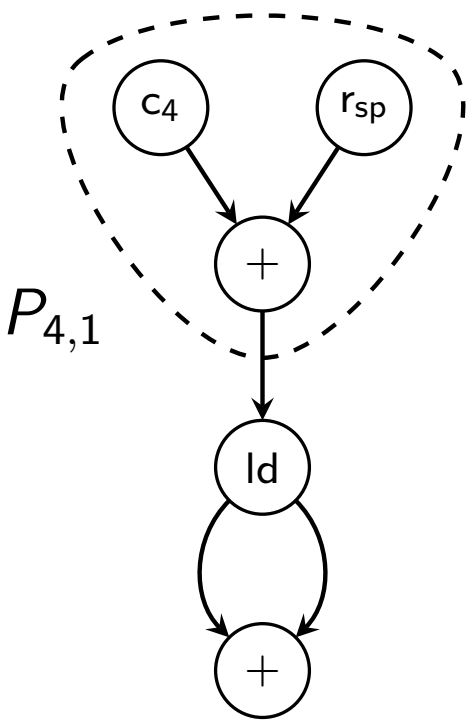

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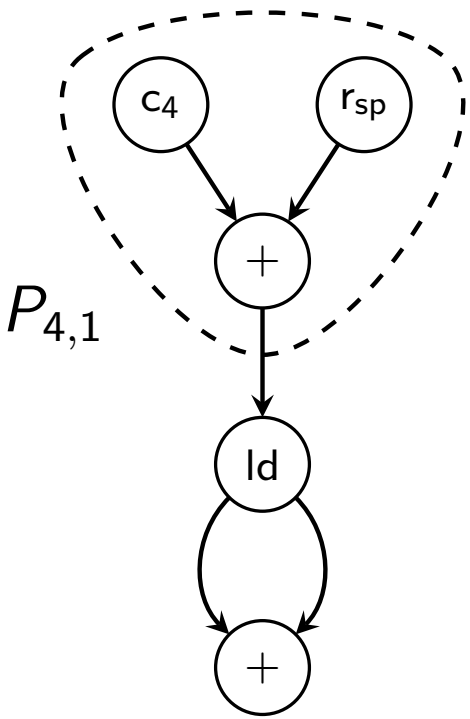

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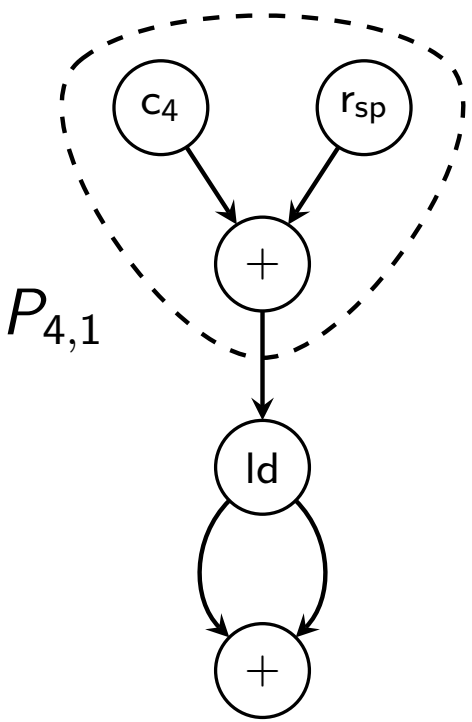

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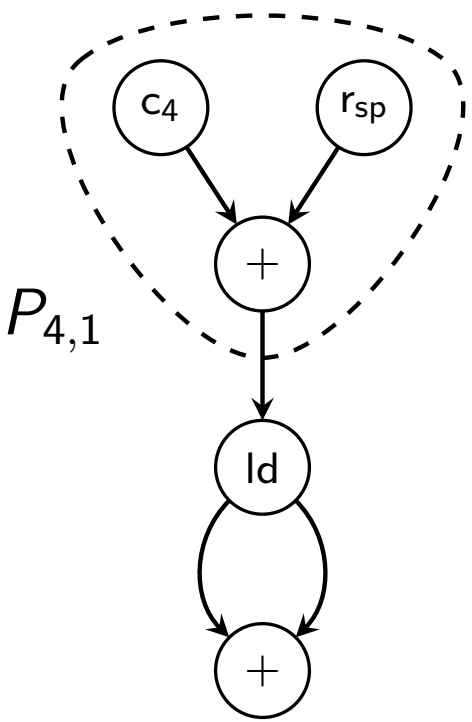
$$D(\boxed{+}) = P_{4,1} \iff D(B_{P_{4,1}}) = 1$$

Instruction Selection



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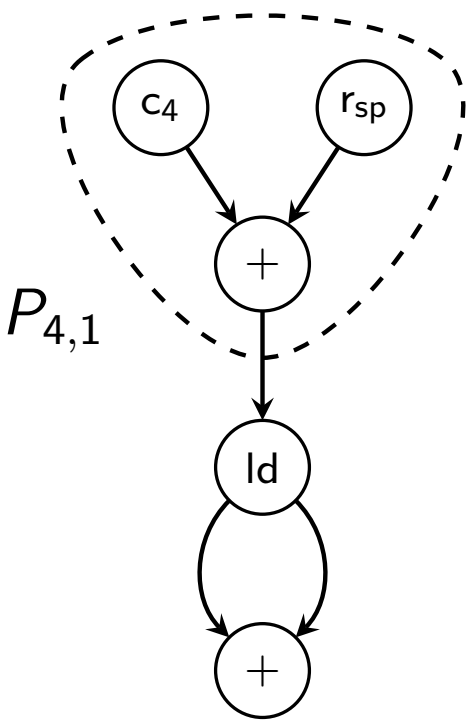
- Objective:

Instruction Selection



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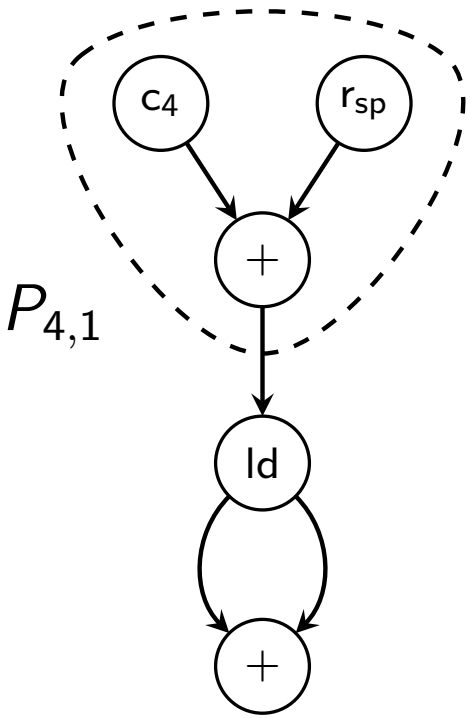
$$D(\textcircled{+}) = P_{4,1} \iff D(B_{P_{4,1}}) = 1$$

- Objective:

$$\min \sum_{p,i \in P_{p,i}} c_p B_{P_{p,i}}$$

Instruction Selection



- Pattern restrictions can simply be added as constraints

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Instruction Scheduling

in which cycle is each instruction issued?

Instruction Scheduling

- Classic scheduling model with:
  - precedences among instructions

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    if i defines a value used by j:

    i must be issued before j

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  - resource constraints

Instruction Scheduling

- Classic scheduling model with:
  - precedences among instructions

    if i defines a value used by j:

    i must be issued before j

  - resource constraints

    if i and j use the same functional unit:

    i and j must be issued in different cycles

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Register Allocation

- Several problems
  - register assignment

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- Several problems
  - register assignment
  - spilling

Register Allocation

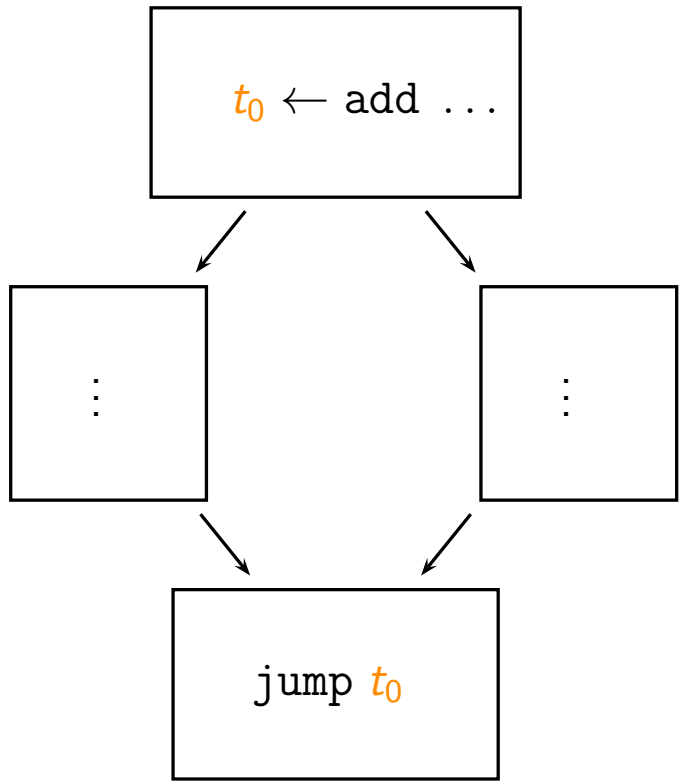
- Several problems
  - register assignment
  - spilling
  - coalescing

Register Allocation

- Several problems
  - register assignment
  - spilling
  - coalescing
- Extra challenge: whole function

Liveness and Interference

- A temp is live while it might still be used:



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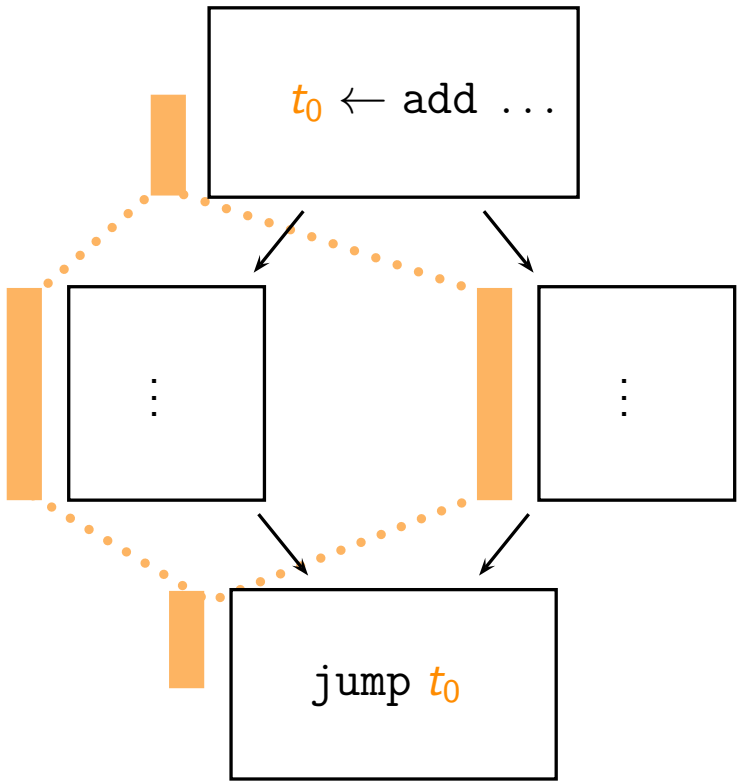

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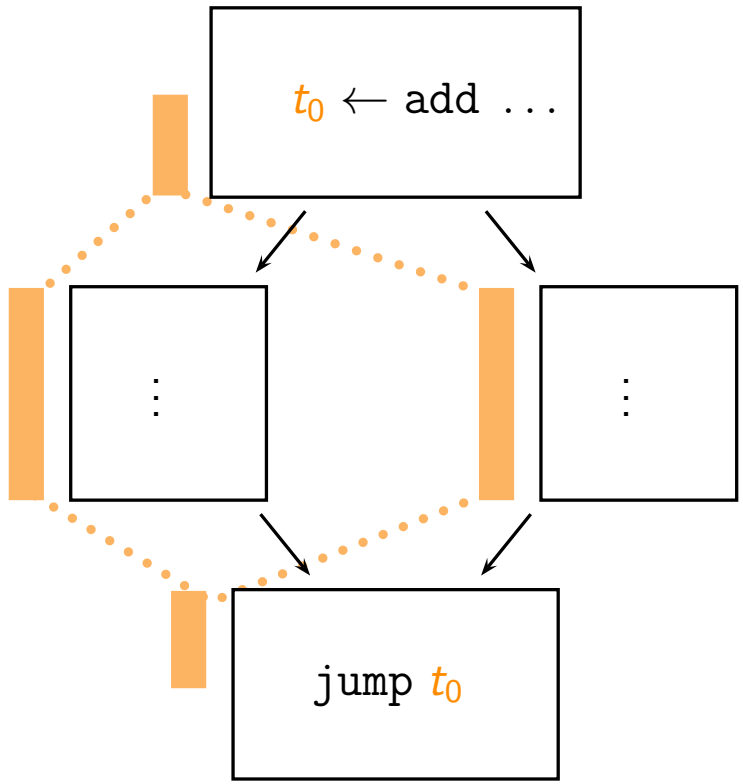

- Two temps interfere if they are live simultaneously

Liveness and Interference

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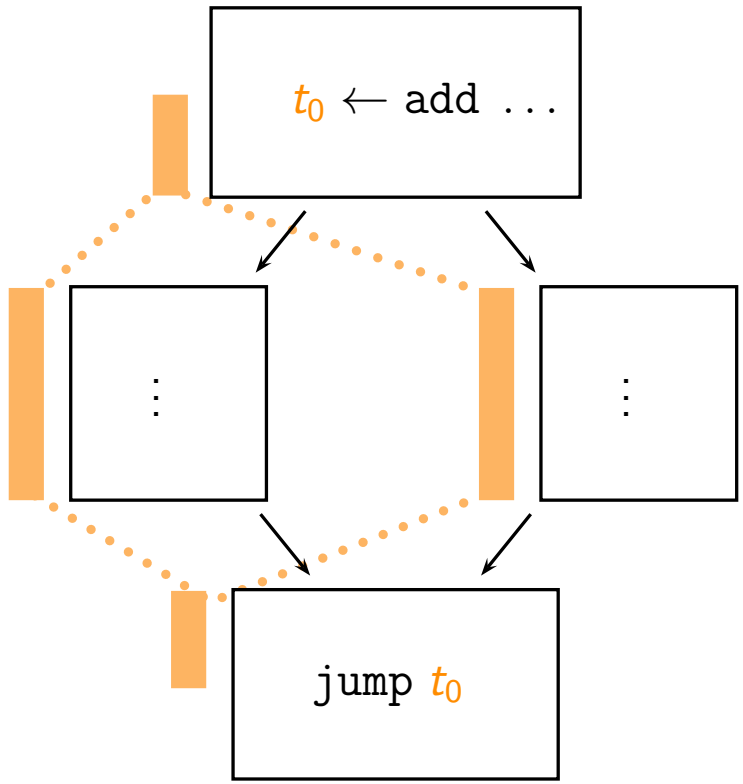

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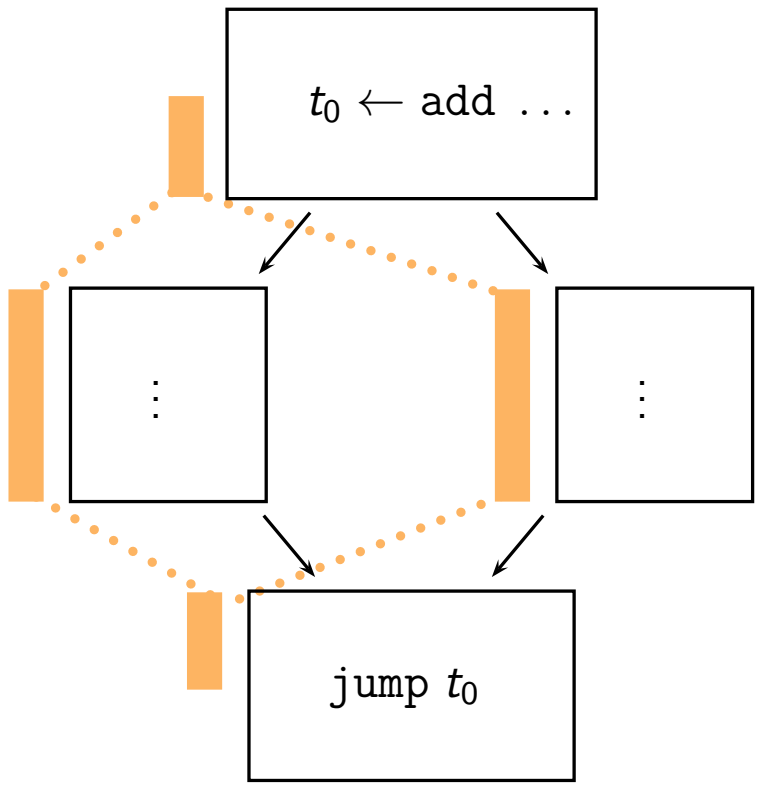

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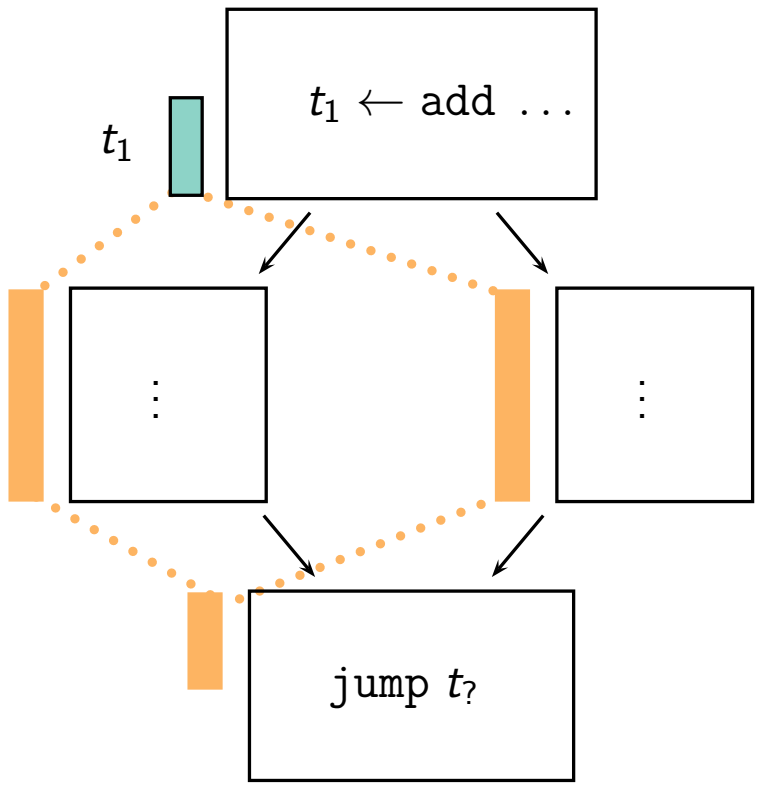

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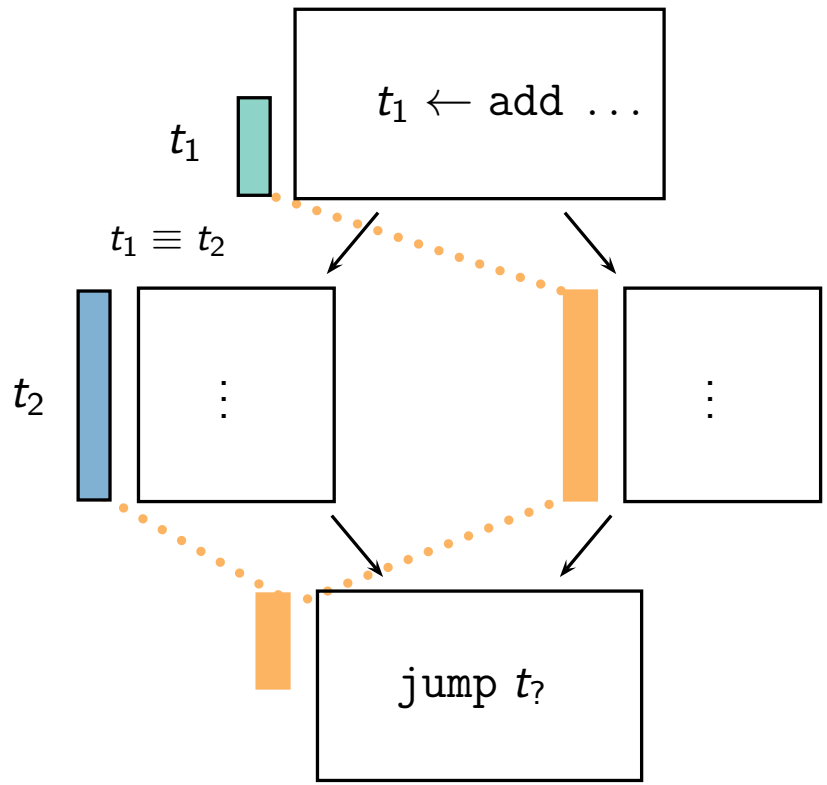

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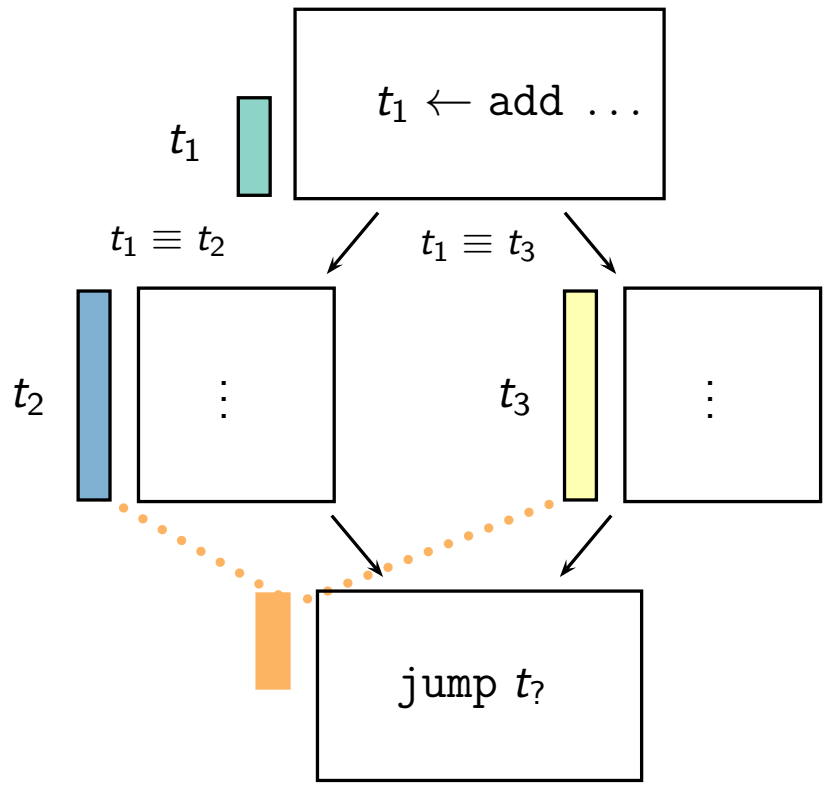

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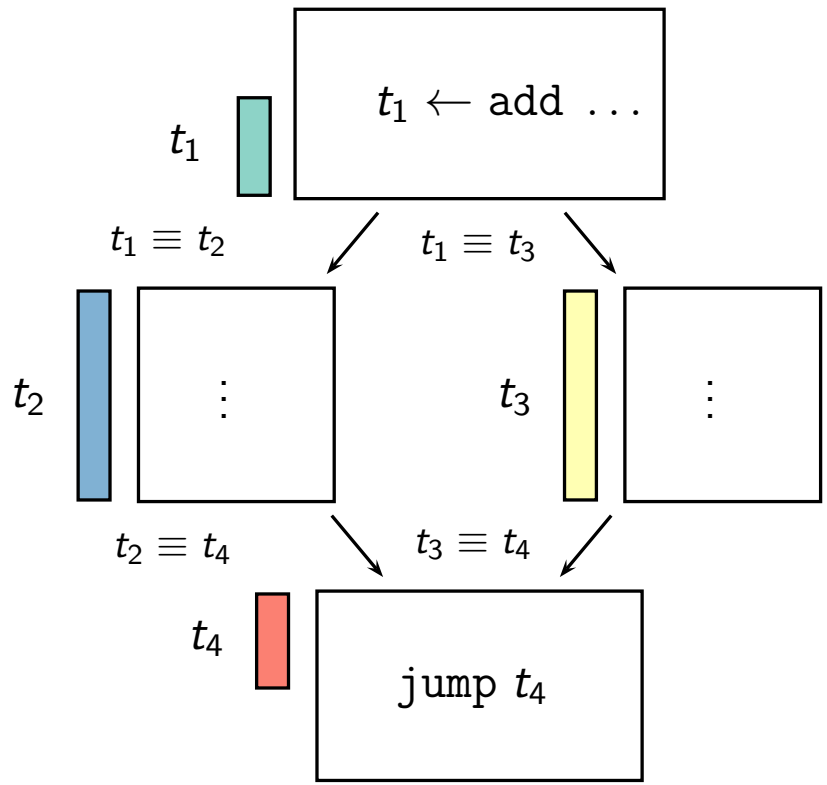

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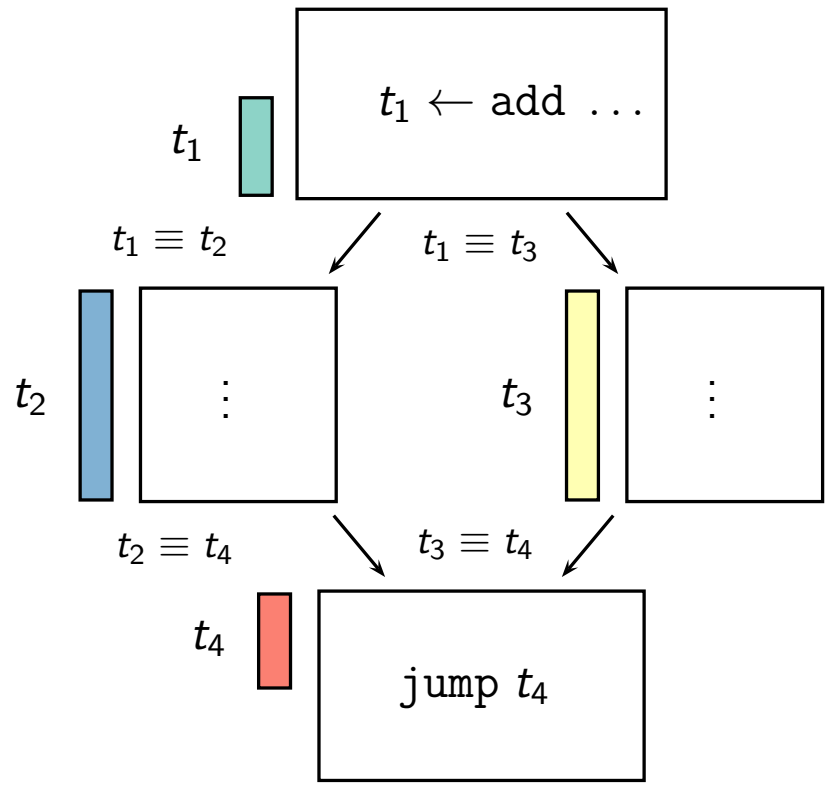

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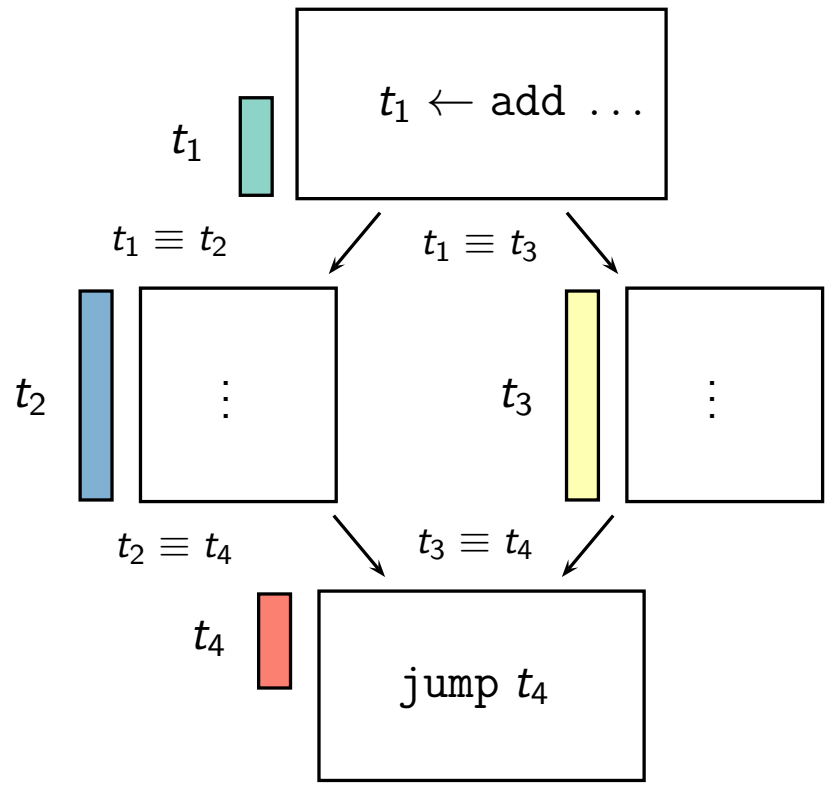

- Invariant: all temps are local $\rightarrow$ simple interference model

Register Assignment

to which register do we assign each temporary?

Register Assignment as Rectangle Packing

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temp live ranges	rectangles

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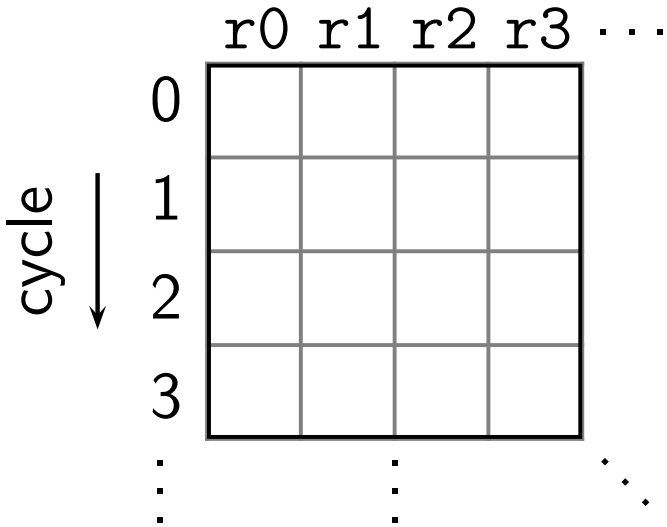

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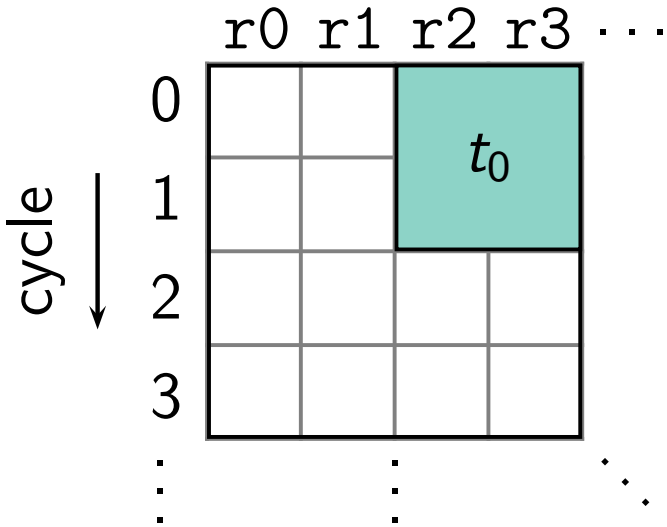

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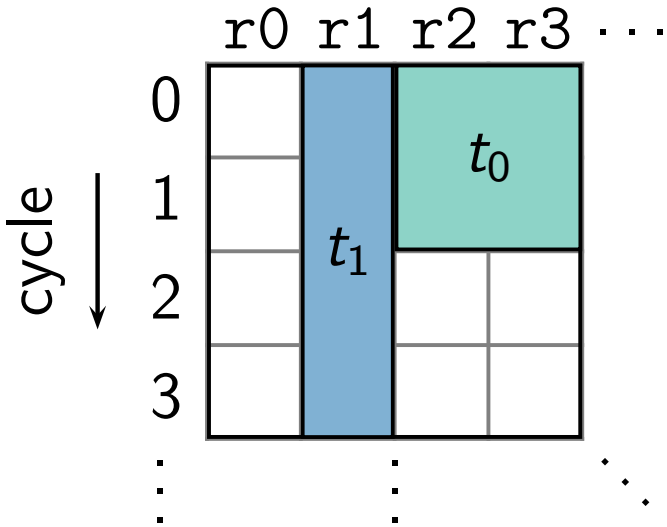

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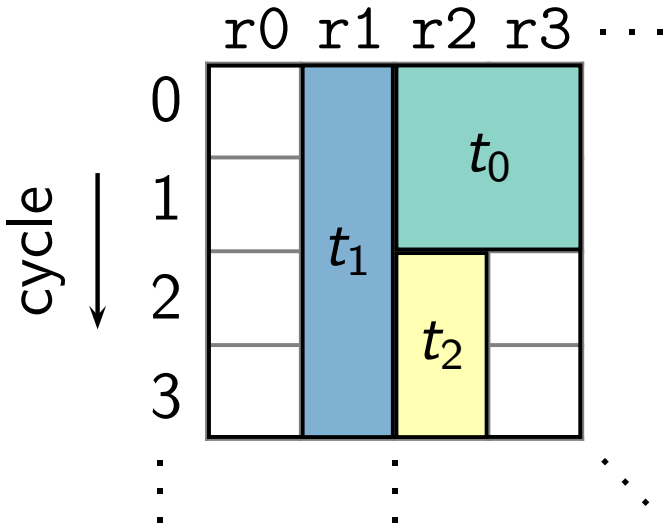

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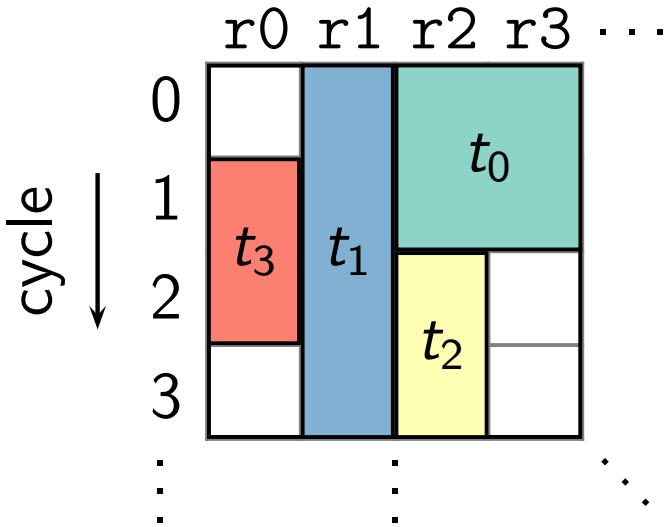

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- Global
  - decomposed temps are assigned to same register

1 Background & Motivation

2 Our Approach

3 Instruction Selection

4 Instruction Scheduling

5 Register Allocation

6 Challenges and Future Work

Overcome Register Allocation Limitations

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  3. if everything else fails, resort to greedy algorithms
     - *decent* polynomial solutions always available